

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## PS21A79 / PS21A7A

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## CHAPTER 1 INTRODUCTION

### 1.1 Target Applications

Motor drives for industrial use, such as packaged air conditioners, general-purpose inverter, servo, except for automotive applications.

### 1.2 Product Line-up

Table 1-1. Line-up

Type Name	IGBT Rating	Motor Rating <sup>(Note 1)</sup>	Isolation Voltage
PS21A79	50A/600V	3.7kW/220V <sub>AC</sub>	V <sub>iso</sub> = 2500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS21A7A	75A/600V	5.5kW/220V <sub>AC</sub>	

Note 1: These motor ratings are general ratings, so those may be changed by conditions.

### 1.3 Functions and Features

Large DIIPM Ver.4 is a compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC100-200V class low power motor inverter control. Fig.1-1, Fig.1-2 and Fig.1-3 show the outline photograph, internal cross-section structure and the circuit block diagram respectively.

One of the most important features of Large DIIPM Ver.4 is that it realized higher thermal dissipation by incorporating thermal structure with high thermal conductive insulated sheet, so that the chip shrink became possible and achieved higher current rating up to 75A than previous Large DIIPM Ver.3 series despite almost same package size.

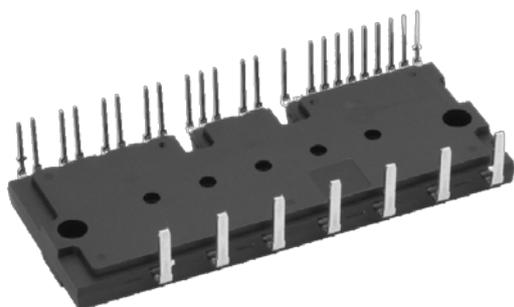


Fig.1-1 Package photograph

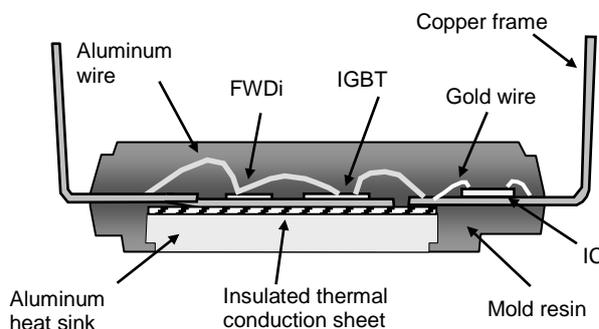


Fig.1-2 Internal cross-section structure

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**Features:**

- For P-side IGBTs
  - Drive circuit
  - High voltage level shift circuit
  - Control supply under voltage (UV) protection circuit (without fault signal output)
- For N-side IGBTs
  - Drive circuit
  - Short circuit (SC) protection circuit (by using external current detecting resistor)
  - Control supply under voltage (UV) protection circuit (with fault signal output)
  - Analog output of LVIC temperature
- Fault Signal Output
  - Corresponding to SC protection and N-side UV protection
- IGBT Drive Supply
  - Single DC15V power supply
- Control Input Interface
  - High active logic
- UL recognized
  - UL1557 File E80276

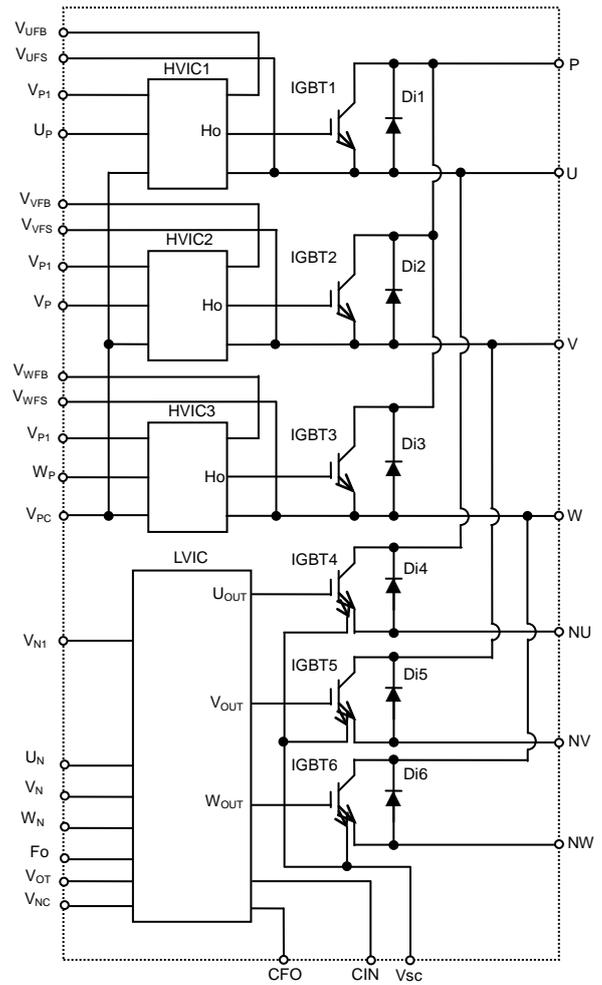


Fig.1-3 Internal circuit schematic

## 1.4 The differences of previous series (Large DIIPM Ver.3 PS2186X) and this series

(1) Enlargement of maximum current rating to 75A

Due to change its insulation structure from mold resin insulation to insulated thermal dissipation sheet, it became possible to decrease the thermal resistance between junction and case  $R_{th(j-c)}$  substantially. So that despite almost same package size, it realized higher current rating up to 75A than previous Large DIIPM Ver.3 series.

(2) Changing the method of short circuit protection (SC)

In the previous series the shunt resistor was inserted between N terminal and power GND line for detecting short circuit current. But the loss at the resistor escalates with increasing current rating, so high wattage type resistor is needed. In this series, the current detection method was changed to the one of detecting slight sense current divided from main current by using on-chip current sense IGBTs. So that the shunt resistor inserted to main flow path for SC protection is unnecessary. For more detail, refer [Section 2.2.1](#).

(3) Analog output function of LVIC temperature

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC and output it by analog signal. But the heat generated at IGBT and FWDi transfers to LVIC through the mold package and the inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current)

It is able to replace the thermistor which was set on outer heat sink with this function. For more detail, refer [Section 2.2.3](#).

(4) Terminal layout

Because of above (2), (3) functions addition and divided N-side IGBT emitter, the terminal layout was changed from Large DIIPM Ver.3 series.

For more detail, refer [Section 2.3](#).

## CHAPTER2 SPECIFICATIONS AND CHARACTERISTICS

### 2.1 Specifications

The specifications are described below by using PS21A7A (75A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

#### 2.1.1 Maximum Ratings

The maximum ratings of PS21A7A are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS21A7A

MAXIMUM RATINGS ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)  
INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC}$	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(\text{surge})}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
$V_{CES}$	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$	75	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$ , up to 1ms	150	A
$P_C$	Collector dissipation	$T_C = 25^\circ\text{C}$ , per 1 chip	162	W
$T_j$	Junction temperature		-20~+150	$^\circ\text{C}$

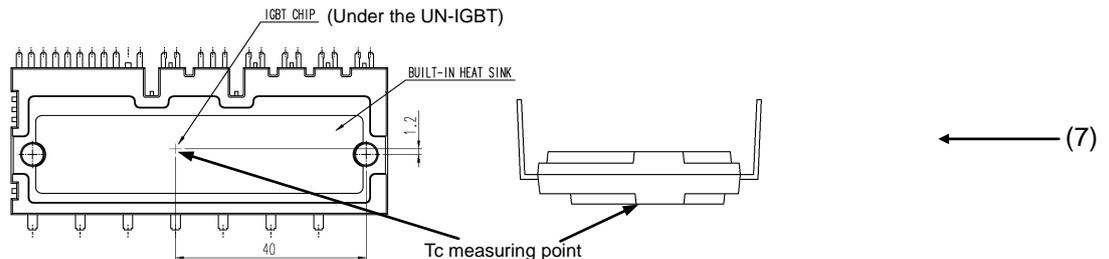
#### CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{PC}$ , $V_{N1}-V_{NC}$	20	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	20	V
$V_{IN}$	Input voltage	Applied between $U_P$ , $V_P$ , $W_P-V_{PC}$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
$V_{FO}$	Fault output supply voltage	Applied between $F_O-V_{NC}$	-0.5~ $V_D+0.5$	V
$I_{FO}$	Fault output current	Sink current at $F_O$ terminal	1	mA
$V_{SC}$	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

#### TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(\text{PROT})}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$ , Inverter Part $T_j = 125^\circ\text{C}$ , non-repetitive, up to 2 $\mu\text{s}$	800	V
$T_C$	Module case operation temperature	(Note 1)	-20~+100	$^\circ\text{C}$
$T_{\text{stg}}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{\text{iso}}$	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	$V_{\text{rms}}$

Note 1:  $T_c$  measurement point



#### [Item explanation]

- (1)  $V_{CC}$  The maximum P-N voltage in no switching state. A voltage suppressing circuit such as a brake circuit is necessary if the voltage exceeds this value.
- (2)  $V_{CC(\text{surge})}$  The maximum P-N surge voltage in switching state. A snubber circuit is necessary if the voltage exceeds  $V_{CC(\text{surge})}$ .
- (3)  $V_{CES}$  The maximum sustained collector-emitter voltage of built-in IGBT.
- (4)  $\pm I_C$  The allowable DC current continuously flowing at collect electrode (@ $T_C=25^\circ\text{C}$ )
- (5)  $T_j$  The maximum junction temperature rating is  $150^\circ\text{C}$ . But for safe operation, it is recommended to limit the average junction temperature up to  $125^\circ\text{C}$ . Repetitive temperature variation  $\Delta T_j$  affects the life time of power cycle, so refer life time curves (Section 3.1.10) for safety design.
- (6)  $V_{CC(\text{prot})}$  The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this rating.
- (7)  $T_c$  position  $T_c$  (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest  $T_c$  point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

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## 2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS21A7A.

Table 2-2 Thermal resistance of PS21A7A

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	-	-	0.77	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	1.25	K/W

Note 2: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about 0.2K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1.  $Z_{th(j-c)}^*$  is the normalized value of the transient thermal impedance. ( $Z_{th(j-c)}^* = Z_{th(j-c)} / R_{th(j-c)max}$ ) For example, the IGBT transient thermal impedance of PS21A7A in 0.1s is  $0.77 \times 0.53 = 0.41K/W$ .

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (E.g. In the cases at motor starting, at motor lock...)

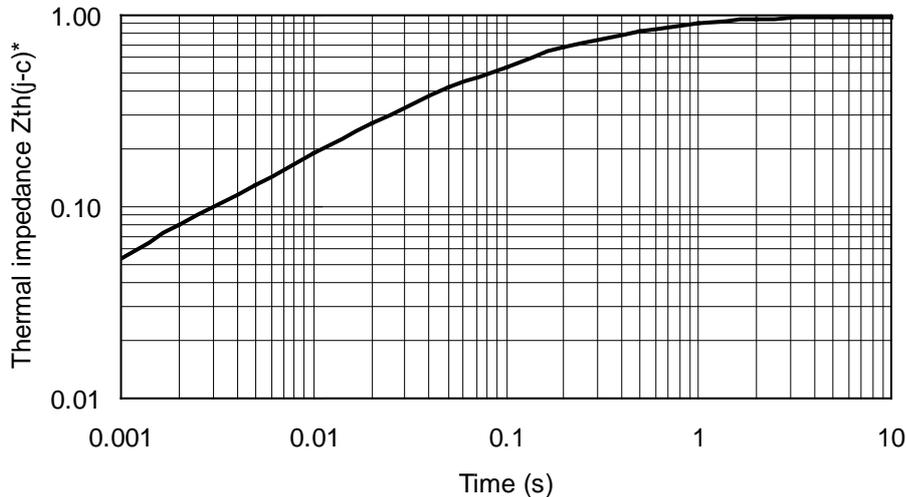


Fig.2-1 Typical transient thermal impedance

## 2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS21A7A.

Table 2-3. Static characteristics and switching characteristics of PS21A7A

Inverter Part

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15V$ $V_{IN} = 5V, I_C = 75A$	$T_j = 25^\circ C$	-	1.55	2.05	V
			$T_j = 125^\circ C$	-	1.65	2.10	
$V_{EC}$	FWDi forward voltage	$-I_C = 75A, V_{IN} = 0V$	-	1.70	2.20	V	
$t_{on}$	Switching times	$V_{CC} = 300V, V_D = V_{DB} = 15V$ $I_C = 75A, T_j = 125^\circ C, V_{IN} = 0 \leftrightarrow 5V$ Inductive Load (upper-lower arm)	-	1.80	2.40	3.60	μs
$t_{C(on)}$			-	0.40	0.60	μs	
$t_{off}$			-	3.40	4.80	μs	
$t_{C(off)}$			-	0.60	1.20	μs	
$t_{rr}$			-	0.30	-	μs	
$I_{CES}$	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	$T_j = 25^\circ C$	-	-	1	mA
			$T_j = 125^\circ C$	-	-	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

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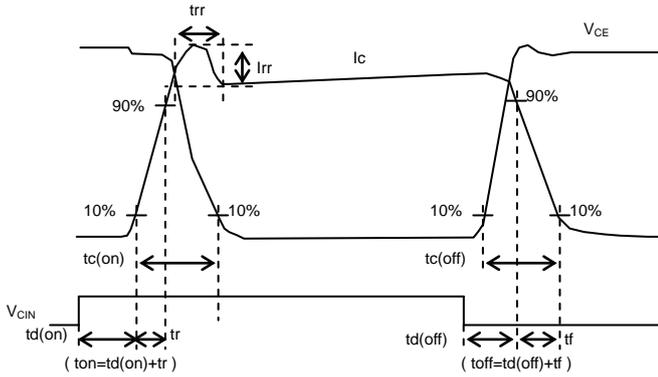


Fig.2-2 Switching time definition

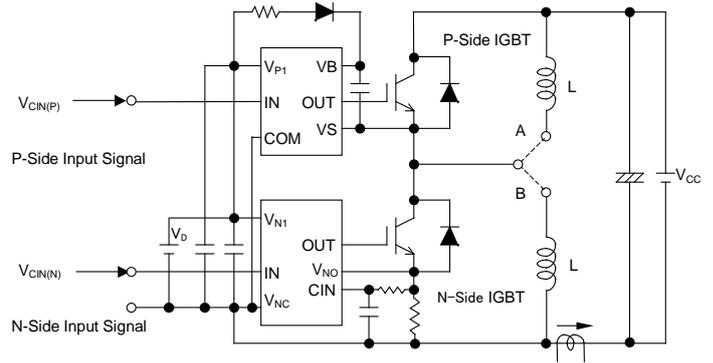


Fig.2-3 Evaluation circuit (inductive load)  
Short A for N-side IGBT, and short B for P-side IGBT evaluation

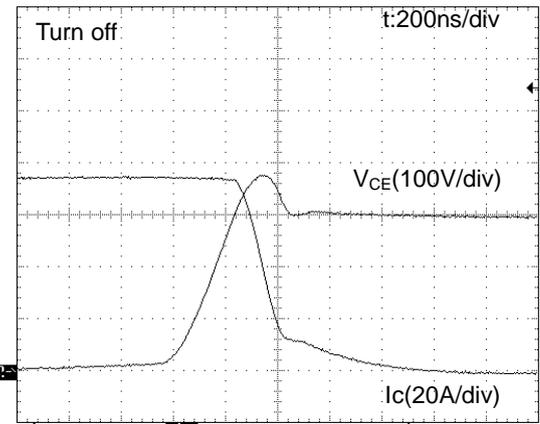
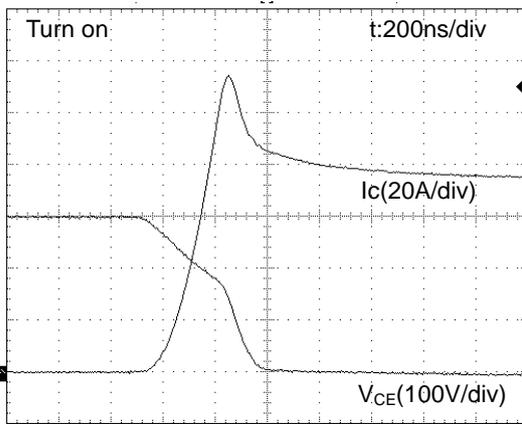


Fig.2-4 Typical switching waveform (PS21A7A)

Conditions:  $V_{CC}=300V$ ,  $V_D=V_{DB}=15V$ ,  $T_j=125^\circ C$ ,  $I_c=75A$ , Inductive load half-bridge circuit

## 2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS21A7A  
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit		
			Min.	Typ.	Max.			
$I_D$	Circuit current	Total of $V_{P1}-V_{PC}$ , $V_{N1}-V_{NC}$ $V_D = 15V, V_{IN} = 0V$ $V_D = 15V, V_{IN} = 5V$	-	-	5.50	mA		
$I_{DB}$	Circuit current	$V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$ $V_D = V_{DB} = 15V, V_{IN} = 0V$ $V_D = V_{DB} = 15V, V_{IN} = 5V$	-	-	0.55			
$I_{SC}$	Short circuit trip level	$-20^\circ C \leq T_j \leq 125^\circ C$ , $R_s = 23.2\Omega (\pm 1\%)$ , Not connecting outer shunt resistors to NU, NV, NW terminals (Note 3)	127	-	-	A		
$UV_{DBt}$	Control supply under-voltage protection	$T_j \leq 125^\circ C$	P-side	Trip level	10.0	-	12.0	V
$UV_{DBr}$				Reset level	10.5	-	12.5	V
$UV_{Dt}$			N-side	Trip level	10.3	-	12.5	V
$UV_{Dr}$				Reset level	10.8	-	13.0	V
$V_{FOH}$	Fault output voltage	$V_{SC} = 0V$ , $F_O$ terminal pull-up to 5V by 10k $\Omega$	4.9	-	-	V		
$V_{FOL}$		$V_{SC} = 1V, I_{FO} = 1mA$	-	-	0.95	V		
$t_{FO}$	Fault output pulse width	$C_{FO} = 22nF$ (Note 4)	1.6	2.4	-	ms		
$I_{IN}$	Input current	$V_{IN} = 5V$	0.7	1.0	1.5	mA		
$V_{th(on)}$	ON threshold voltage	Applied between $U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}$	2.1	2.3	2.6	V		
$V_{th(off)}$	OFF threshold voltage		0.8	1.4	2.1	V		
$V_{OT}$	Temperature output	LVIC temperature = 85 $^\circ C$ (Note 5)	3.57	3.63	3.69	V		

Note 3 : Short circuit protection can work for N-side IGBTs only.  $I_{SC}$  level can change by sense resistance. For details, please refer the application note for this DIIPM or contact us. And in that case, it should be for sense resistor to be larger resistance than the value mentioned above.

4 : Fault signal is output when short circuit or N-side control supply under-voltage protective functions operate. The fault output pulse-width  $t_{FO}$  depends on the capacitance value of  $C_{FO}$ . ( $C_{FO} (typ.) = t_{FO} \times (9.1 \times 10^6) [F]$ )

5 : DIIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIIPM. And this output might exceed 5V when temperature rises excessively, so it is recommended for protection of control part like MCU to insert a clamp Di between supply (e.g. 5V) for control part and this output.

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## 2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS21A7A are given in Table 2-5. Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIIPM safe operation.

Table 2-5 Recommended operating conditions of PS21A7A  
RECOMMENDED OPERATION CONDITIONS

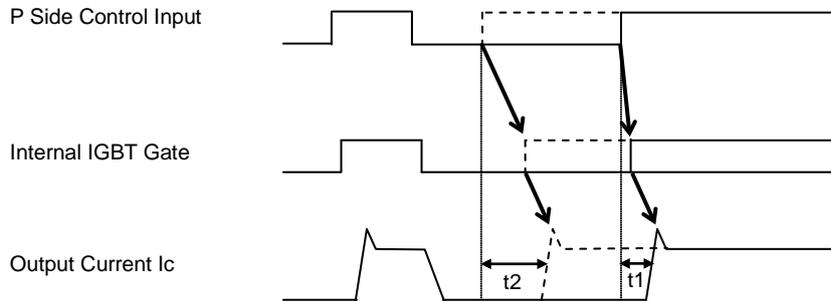
Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V	
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{PC}$ , $V_{N1}-V_{NC}$	13.5	15.0	16.5	V	
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/ $\mu$ s	
$t_{dead}$	Arm shoot-through blocking time	For each input signal, $T_C \leq 100^\circ\text{C}$	2.7	-	-	$\mu$ s	
$f_{PWM}$	PWM input frequency	$T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$	-	-	20	kHz	
$I_O$	Allowable r.m.s. current	$V_{CC} = 300\text{V}$ , $V_D = 15\text{V}$ , P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$ (Note 7)	$f_{PWM} = 5\text{kHz}$	-	-	35.0	Arms
			$f_{PWM} = 15\text{kHz}$	-	-	17.0	
PWIN(on)	Minimum input pulse width	$200 \leq V_{CC} \leq 350\text{V}$ , $13.5 \leq V_D \leq 16.5\text{V}$ , $13.0 \leq V_{DB} \leq 18.5\text{V}$ , $-20^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$ , N line wiring inductance less than 10nH (Note 9)	(Note 8)	1.3	-	-	$\mu$ s
PWIN(off)			$I_C \leq 75\text{A}$	3.0	-	-	
			$75 < I_C \leq 127.5\text{A}$	5.0	-	-	
$V_{NC}$	$V_{NC}$ variation	Between $V_{NC}-\text{NU}$ , NV, NW (including surge)	-5.0	-	+5.0	V	
$T_J$	Junction temperature		-20	-	+125	$^\circ\text{C}$	

Note 7: The allowable r.m.s. current value depends on the actual application conditions.

8: DIIPM might not make response to the input on signal with pulse width less than PWIN (on).

9: DIIPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Refer below about delayed response.

### Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width > PWIN(off); turn on time  $t_1$   
 Broken line: off pulse width < PWIN(off); turn on time  $t_2$   
 ( $t_1$ : Normal switching time)

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## 2.1.6 Mechanical Characteristics and Ratings

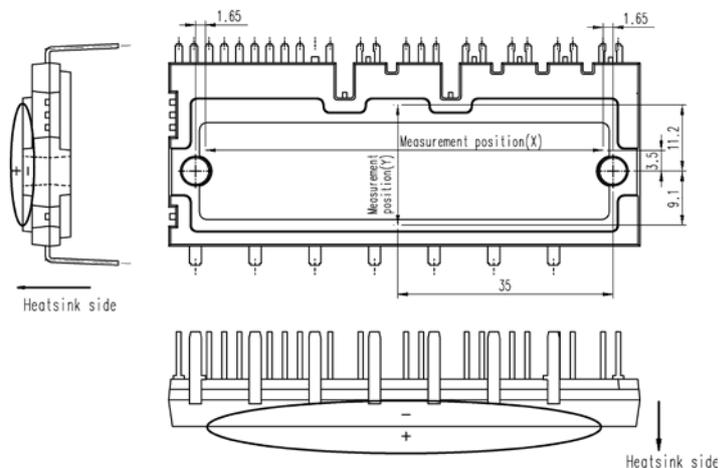
The mechanical characteristics and ratings are shown in Table 2-6  
Please refer to Section 2.4 for the detailed mounting instruction.

Table 2-6 Mechanical characteristics and ratings of PS21A7A

### MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	Load 19.6N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Load 9.8N, 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	46	-	g
Heat-sink flatness			-50	-	100	μm

Measurement point of heat-sink flatness



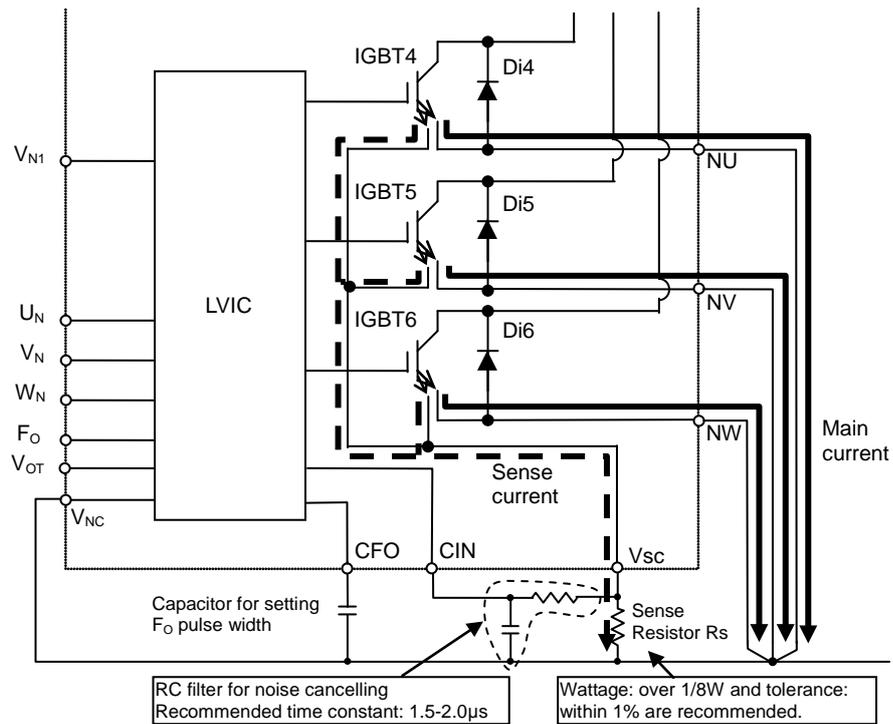
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## 2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and outputting LVIC temperature function in the large DIIPM Ver.4. The detailed information are described below.

### 2.2.1 Short Circuit Protection

In large DIIPM Ver.4 series, the method of SC protection is different from DIIPM Ver.3 series, which detects main current by shunt resistor inserted into main current path. It detects much smaller sense current, which is split at N-side IGBT, by measuring the potential of sense resistor connected to Vsc terminal. So high wattage type shunt resistor isn't necessary for SC protection, and the loss at shunt resistor can be reduced. (Fig.2-5)



\*) This wattage of sense resistor is described as a guide, so it is recommended to evaluate on your real system well.

Fig.2-5 SC protection circuit

SC protection works by inputting the potential, which is generated by sense current flowing into the sense resistor, to the CIN terminal. When SC protection works, DIIPM shuts down all N-side IGBTs and outputs F<sub>O</sub> signal. (Its pulse width(t<sub>F<sub>O</sub></sub>) is set by C<sub>F<sub>O</sub></sub> capacitor.  $C_{F_O} = t_{F_O} \times 9.1 \times 10^{-6}$  [F]) Table 2-7 describes specified sense resistance and minimum SC protection current in that case for each products.

To prevent malfunction, it is recommended to insert RC filter before inputting to CIN terminal and set the time constant to shut down within 2µs when short circuit occurs. (Time constant 1.5µ-2.0µs is recommended.) Also it is necessary to set the resistance of RC filter to ten or more times of the sense resistor R<sub>s</sub>. (Hundred times is recommended.)

Table 2-7 SC protection trip level (Condition: T<sub>J</sub>=-20°C~125°C, Not connecting outer shunt resistors to NU, NV, NW terminals.)

	R <sub>s</sub>	Min.
PS21A7A	23.2Ω	127A
PS21A79	40.2Ω	85A

Sense resistance is set to 23.2Ω for PS21A7A and 40.2Ω for PS21A79 without outer shunt resistors into main current path. For sense resistor, its large fluctuation leads to large fluctuation of SC trip level. So it is necessary to select small variation in the resistance (within +/-1% is recommended)

Wattage of the sense resistor can be estimated in view of the fact that the maximum split ratio between the main and sense currents is about 3000:1 for PS21A7A and PS21A79. (In this case maximum sense current flows.) The estimation example for PS21A7A is described as below.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

[Estimation example]

(1) Normal operation state

It is assumed that the maximum main current for normal operation is 150A (rated current x 2, for keeping a margin) and the sense resistance is 23.2Ω.

In this case, The maximum sense current flows through the sense resistor is calculated as below.

$$150A / 3000 = 50mA$$

And the loss at the sense resistor is

$$P = I^2 \cdot R \cdot t = (50mA)^2 \times 23.2\Omega \times 1s = \underline{58mW}$$

(2) Short circuit state

When short circuit occurs, its current depends on the condition, but up to IGBT saturation current (about 10 times of the rated current =750A) flows. So the sense current is

$$750A / 3000 = 250mA$$

But this current shut down within 2μs by SC protection. And the average loss at the sense resistor is

$$P = I^2 \cdot R \cdot t = (250mA)^2 \times 23.2\Omega \times 2\mu s / 1s = \underline{0.0029mW}$$

As explained above, over 1/8W wattage resistor will be suitable, but it is necessary to confirm on your real system finally.

[Remarks]

It takes more time (Table 2-8) from inputting over threshold voltage to CIN terminal to shutting down IGBTs. (Because of IC's transfer delay)

Table 2-8 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from short circuit occurring to shutting down IGBTs is the sum of the delay by the outer RC filter and this IC delay.

[SC protection (N-side only)]

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger) (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
- a3. All N-side IGBTs' gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo outputs with a fixed pulse width determined by the external capacitance C<sub>FO</sub>.
- a6. Input "L": IGBT off.
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

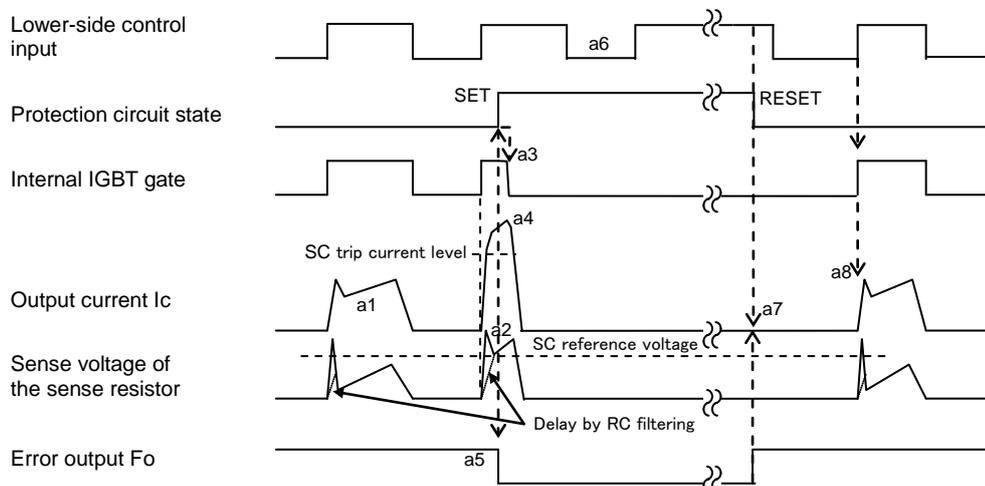


Fig.2-6 SC protection timing chart

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[About Short Circuit Protection by Sense IGBT]

This function aims to protect from Short Circuit like arm short or load short. If high accuracy of protection current level (e.g. demagnetizing current of motor) is necessary, it is recommended to adopt the method by detecting the voltage at outer shunt resistors into main current path. In that case, the current split ratio between main and sense currents varies, thus minimum SC protection trip level changes from the value in Table 2-7. Therefore, adjustment of the sense resistance will be needed. The example of minimum SC trip level with outer shunt resistor is described in Table 2-9. (PS21A79, at sense resistance 40.2Ω) Please contact us about selecting sense resistance in the case of inserting outer shunt resistors.

It is recommended to set outer shunt resistance 7mΩ or less for PS21A79 and 4.5mΩ or less for PS21A7A because too large shunt resistance causes a decrease of IGBT saturation current by decreasing gate voltage at large current. (Large current makes large voltage drop at shunt resistor.) For shunt resistor, select the low parasitic inductance resistor like surface mounted device type and pattern the wiring from the N-side emitter (NU, NV, NW) terminals as short as possible because of reducing surge by shutdown at large short circuit current.

Table 2-9 SC protection trip level (PS21A79, sense resistance 40.2Ω)

Outer shunt resistance	Minimum SC trip level
Nothing	85A
3mΩ	57A
5mΩ	48A

As a method that combines short circuit and over current protection function, there is a method which doesn't use sense resistor too. It is the same method as former DIIPM Ver.3 and the example of the protection circuit is described in Fig.2-7.

The SC protection trip level is needed to set to double the rated current or less. And it is recommended to set the reference voltage of comparators to about 0.5V and select the shunt resistance in order that the SC trip level may be double the rated current or less. (E.g. for PS21A79 (rated current 50A),  $R=0.5V/100A=5m\Omega$  or more)

When this protection method is applied, the rated sense resistor should be connected between Vsc terminal and GND for protecting from surge too. (Don't leave it open.)

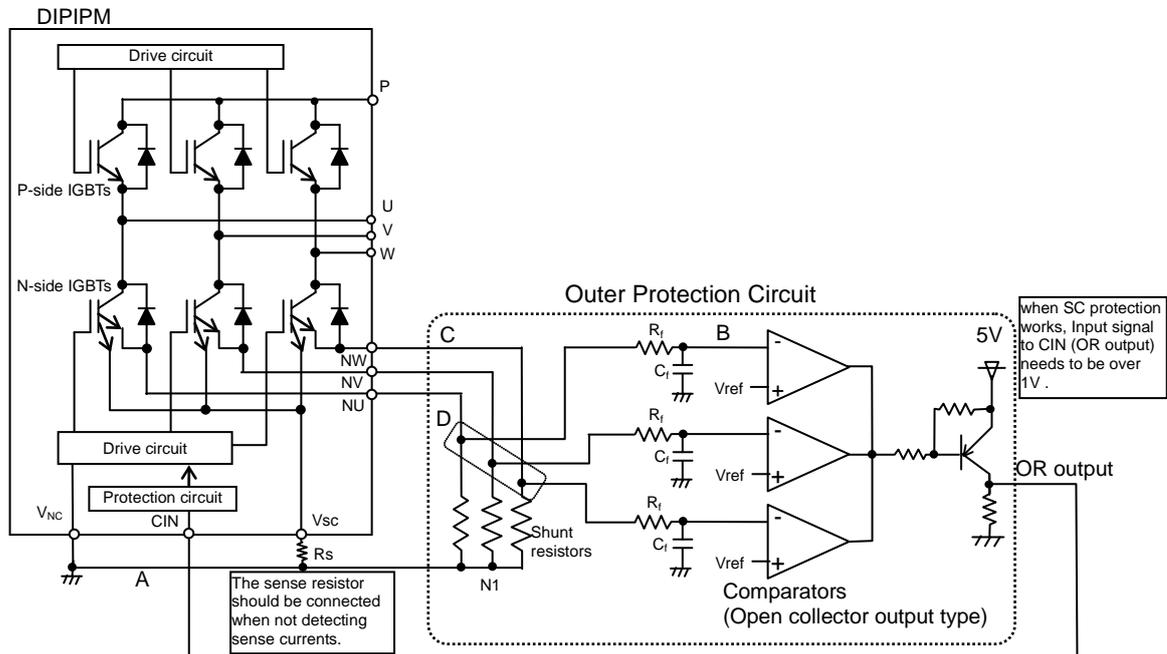


Fig.2-7 Example of SC protection circuit without detecting sense current.

**Note:**

- It is necessary to set the time constant  $R_f C_f$  of external comparator input so that IGBT can stop within  $2\mu s$  when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on. If additional RC filter is inserted into OR output, it is necessary to consider its delay too.
- The threshold voltage  $V_{ref}$  is recommended to set about 0.5V.
- Select the shunt resistance so that SC trip-level is less than double the rated current.
- To avoid malfunction, the wiring A, B, C should be as short as possible.
- The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- OR output high level should be over 1V.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 2.2.2 Control Supply UV Protection

The UV protection is designed for preventing unexpected operating behavior as described in Table 2-10.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10µs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10µs after UV happened.

Table 2-10 DIIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIIPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on. (Avoid inputting ON-signals to DIIPM before the control supply coming up to 13.5V)
4.0-UV trip level (P, N)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV trip level-13.5V(N),13.0V(P)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions. (Normal operation)
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	Over maximum voltage rating. The control circuit will be destroyed.

### Ripple Voltage Limitation of Control Supply

If high frequency precipitous noise is superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, \quad V_{ripple} \leq 2Vp-p$$

### N-side UV Protection Sequence

- a1. Control supply voltage  $V_D$  exceeds under voltage reset level ( $UV_{Dr}$ ), but IGBT turns ON when inputting next ON signal (L→H). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a2. Normal operation: IGBT turn on and carry current.
- a3.  $V_D$  level drops to under voltage trip level. ( $UV_{Dt}$ ).
- a4. All N-side IGBTs turn OFF in spite of control input condition.
- a5. Fo outputs for the period determined by the capacitance  $C_{FO}$ , but output is extended during  $V_D$  keeps below  $UV_{Dr}$ .
- a6.  $V_D$  level reaches  $UV_{Dr}$ .
- a7. Normal operation: IGBT ON and carry current.

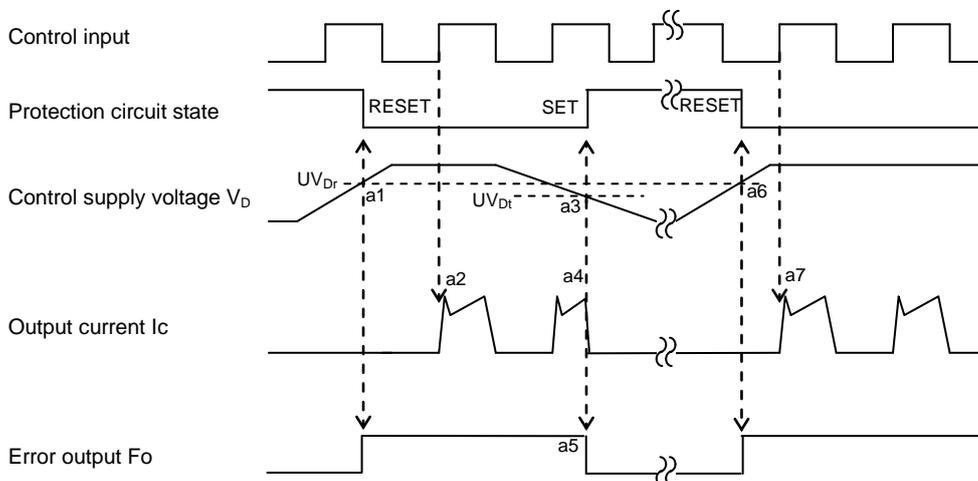


Fig.2-8 Timing chart of N-side UV protection

### P-side UV Protection Sequence

- b1. Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBr}$ , IGBT can turn on when inputting next ON signal (L→H).
- b2. Normal operation: IGBT ON and outputs current.
- b3.  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBt}$ ).
- b4. IGBT of corresponding phase only turns OFF in spite of control input signal level, but there is no  $F_O$  signal output.
- b5.  $V_{DB}$  level reaches  $UV_{DBr}$ .
- b6. Normal operation: IGBT ON and carry current.

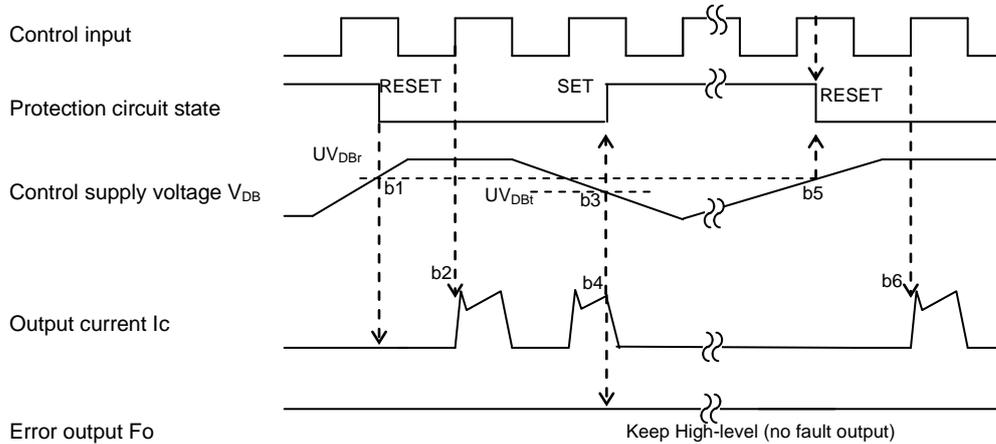


Fig.2-9 Timing Chart of P-side UV protection

### 2.2.3 Temperature analog output

#### (1) Purpose of this function

This function measures the temperature of control LVIC by built in temperature detecting circuit on LVIC. The heat generated at IGBT and FWDi transfers to LVIC through mold package and inner and outer heat sink. So that LVIC temperature cannot respond to rapid temperature change of those power chips effectively. (e.g. motor lock, short current) It is recommended to use this function for protecting from excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was set on outer heat sink currently)

#### [Note]

DIIPM cannot shutdown IGBT and output fault signal automatically when temperature rises excessively. When temperature exceeds the defined protect level, controller (MCU) should stop the DIIPM.

#### (2) $V_{OT}$ characteristics

Inner circuit of  $V_{OT}$  terminal is the output of OP amplifier circuit and is described as Fig.2-10

If the resistor is inserted between  $V_{OT}$  and  $V_{NC}$ (control supply GND) terminals, then the current (calculated by  $V_{OT}$  output ÷ resistance of inserted resistor) always flows as circuit current of LVIC.

The current capability of  $V_{OT}$  output is described as Table 2-11.

Table 2-11 Output capability ( $T_c = -20^\circ\text{C} \sim 100^\circ\text{C}$ )

	min.
Source	1.7mA
Sink	0.1mA

Source : the current flow from  $V_{OT}$  to outside.

Sink : the current flow from outside to  $V_{OT}$ .

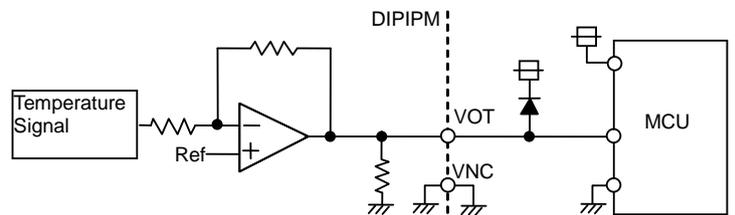


Fig.2-10 Inner circuit of  $V_{OT}$  terminal

This output might exceed 5V when temperature rises excessively, so it is recommended for protection of control part like MCU to insert a clamp Di between supply (e.g. 5V) for control part and this output.

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The characteristics of  $V_{OT}$  output vs. LVIC temperature is described as Fig.2-11.

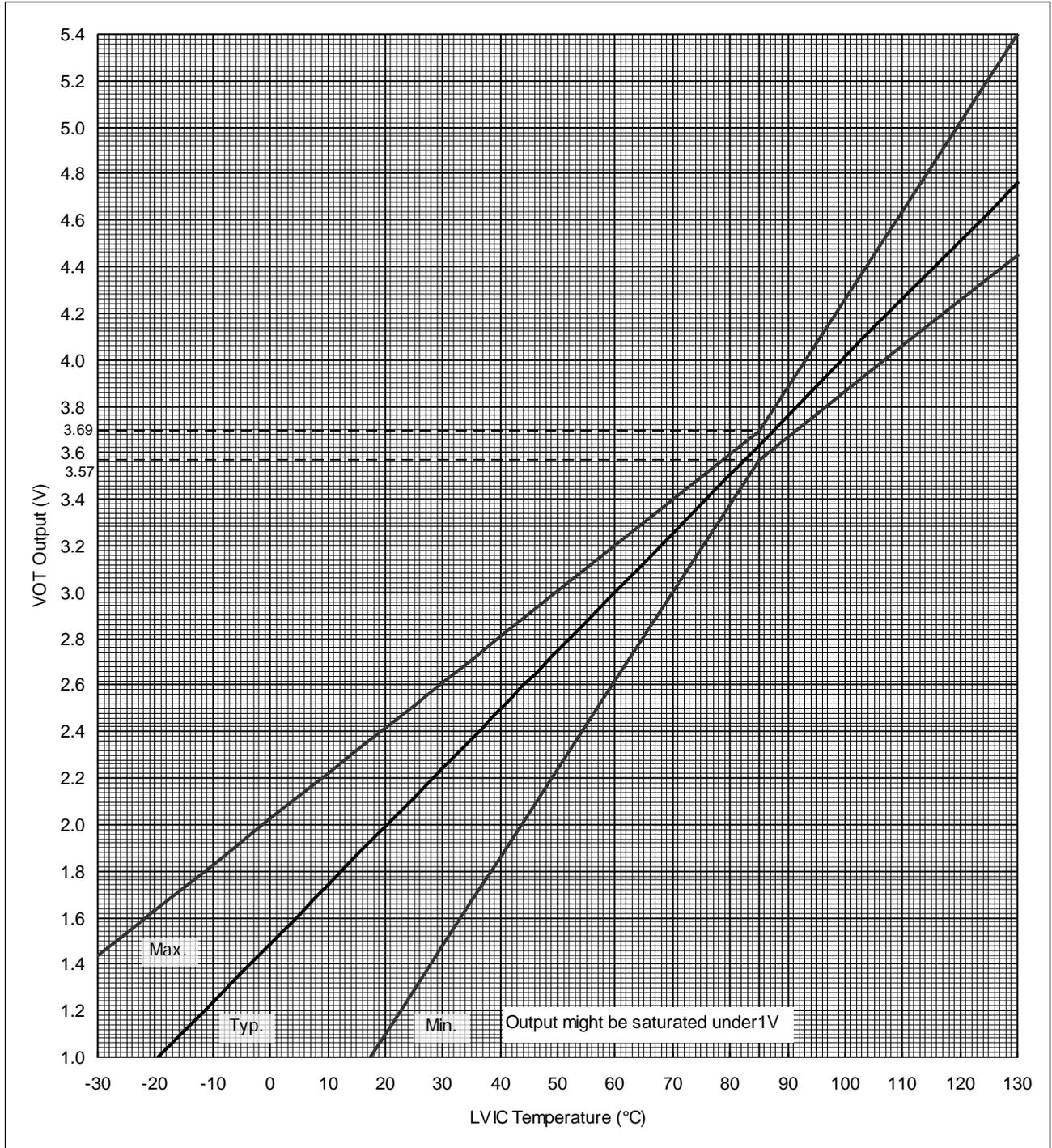


Fig.2-11  $V_{OT}$  output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the package and heat sink, and the relationship between LVIC temperature:  $T_{ic}(=V_{OT}$  output), case temperature:  $T_c$  (measuring point is defined on datasheet), and junction temperature:  $T_j$  depend on the system cooling condition, heat sink, control strategy, etc.

For example, the evaluation results in the case of using different size heat sink (Table 2-12) are described as Fig.2-12. As the result of evaluations, it is clear that two cases have different relationships between LVIC temperature  $T_{ic}$  and case temperature  $T_c$ .

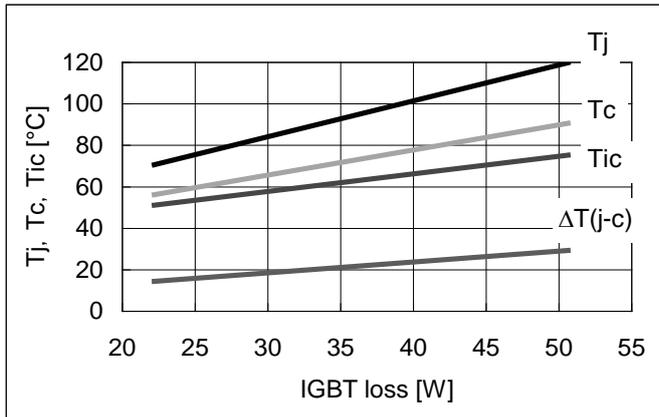
So when setting the threshold temperature for protection, it is necessary to measure the relationship between them on your real system. And when setting threshold temperature  $T_{ic}$ , it is important to consider the protection temperature is at  $T_c \leq 100^\circ\text{C}$  and  $T_j \leq 150^\circ\text{C}$ .

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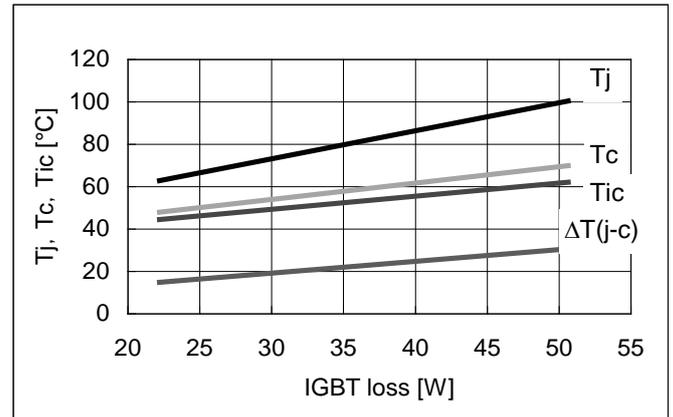
Measuring each temperatures @ only 1 IGBT chip turns on (DC current, Ta=25°C)

Table 2-12 Outer heat sink

	Thermal resistance Rth(f-a)	Heat sink size (L x D x H)
A	2.20K/W	100 x 88 x 40 mm
B	1.35K/W	200 x 88 x 40 mm



(a) Heat sink A



(b) Heat sink B

Fig.2-12 IGBT loss vs. Tj, Tc, Tic(Ta=25°C, Typical)

The procedure example of setting protection temperature is described below.

Fig.2-13 indicates the example of the relationship between LVIC temperature Tic, case temperature Tc and junction temperature Tj, and Fig.2-14 is the relationship between V<sub>OT</sub> and Tc, which is obtained by combining Fig.2-11 and Fig.2-13.

If the protection level is set to Tj=125°C (Tc=100°C), then V<sub>OT</sub> threshold level should be set 3.75V which is the maximum value @ Tc=100°C in Fig.2-14.

In this case the variation of real Tc may become from 100°C to 115°C. But even if the real Tc will be maximum variation value 115°C, Tj becomes under 150°C (125°C+15°C=140°C<150°C).

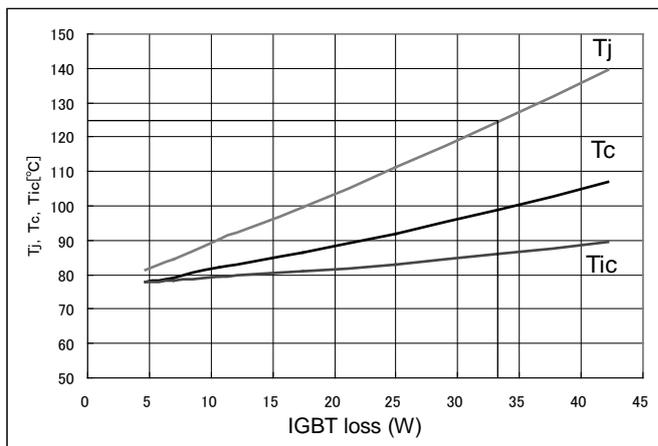


Fig.2-13 IGBT loss vs. Tj, Tc, Tic(Typical) (Ta=80°C)

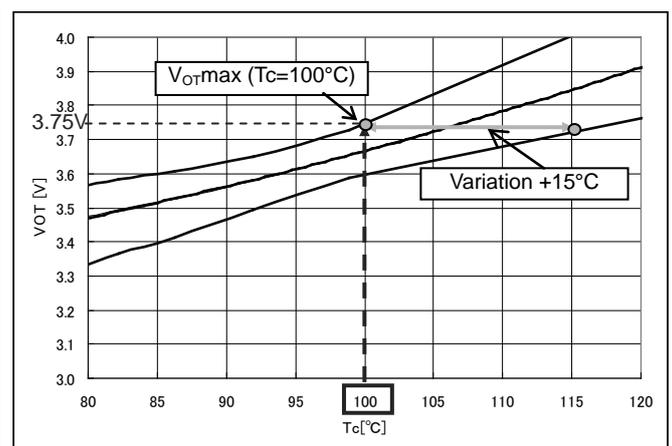


Fig.2-14 V<sub>OT</sub> vs. Tc (Typical)

As mentioned above, the relationship between Tic, Tc and Tj depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V<sub>OT</sub> vs. LVIC temperature.

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## 2.3 Package Outlines

### 2.3.1 Outline Drawing

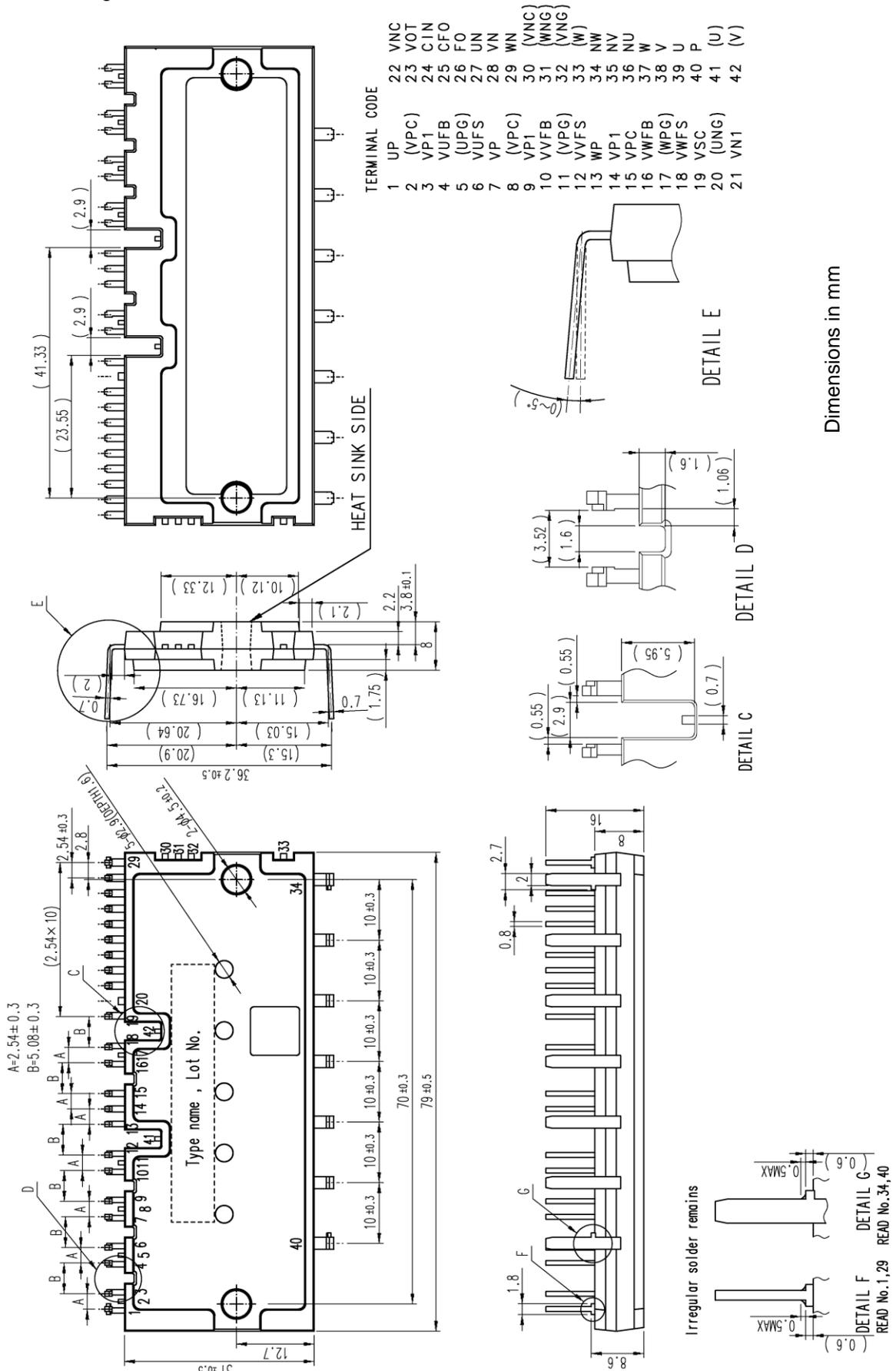


Fig.2-15 Outline drawing

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 2.3.2 Power Chip Position

Fig.2-16 indicates the center position of the each power chips.  
 (This figure is the view from laser marked side.)

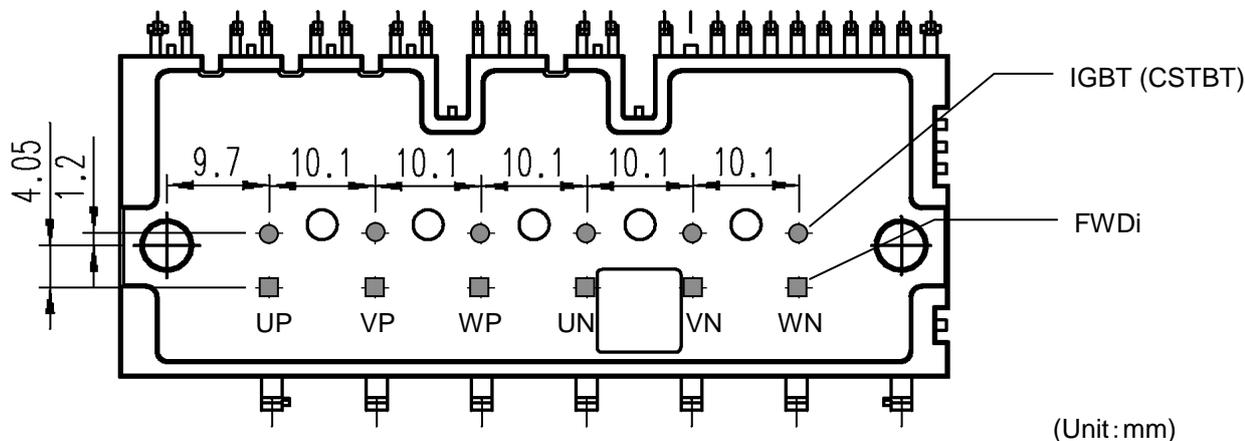
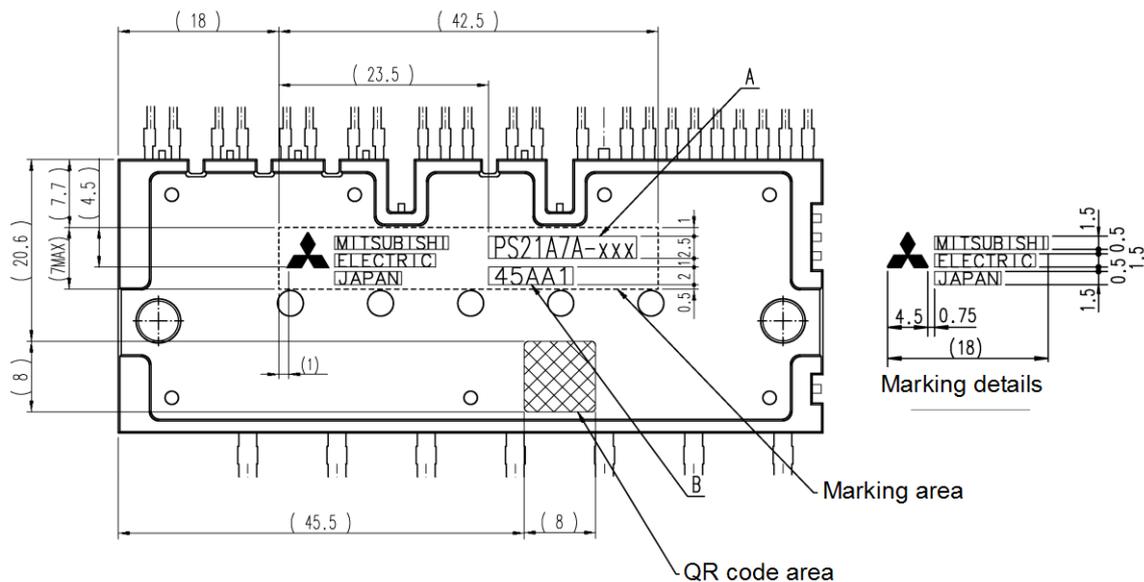


Fig.2-16 Power chip position

## 2.3.3 Laser Marking Position

The laser marking specification is described in Fig.2-17.  
 Mitsubishi Corporation mark, Type name (A), Lot number (B), and QR code mark are marked in the upper side of module.



QR Code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.

Fig.2-17 Laser marking view

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## 2.3.4 Terminal Description

Table 2-13 Terminal description

No.	Name	Description
1	U <sub>P</sub>	U-phase P-side control input terminal
3	V <sub>P1</sub>	U-phase P-side control supply positive terminal
4	V <sub>UFB</sub>	U-phase P-side drive supply positive terminal
6	V <sub>UFS</sub>	U-phase P-side drive supply GND terminal
7	V <sub>P</sub>	V-phase P-side control input terminal
9	V <sub>P1</sub>	V-phase P-side control supply positive terminal
10	V <sub>VFB</sub>	V-phase P-side drive supply positive terminal
12	V <sub>VFS</sub>	V-phase P-side drive supply GND terminal
13	W <sub>P</sub>	W-phase P-side control input terminal
14	V <sub>P1</sub>	W-phase P-side control supply positive terminal
15	V <sub>PC</sub>	P-side control supply GND terminal
16	V <sub>WFB</sub>	W-phase P-side drive supply positive terminal
18	V <sub>WFS</sub>	W-phase P-side drive supply GND terminal
19	V <sub>SC</sub>	Sense current detecting terminal
21	V <sub>N1</sub>	N-side control supply positive terminal
22	V <sub>NC</sub>	N-side control supply GND terminal
23	V <sub>OT</sub>	LVIC temperature output terminal
24	CIN	SC trip voltage detect terminal
25	CFO	Fault pulse output width set terminal
26	F <sub>O</sub>	Fault signal output terminal
27	U <sub>N</sub>	U-phase N-side control input terminal
28	V <sub>N</sub>	V-phase N-side control input terminal
29	W <sub>N</sub>	W-phase N-side control input terminal
34	NW	W-phase N-side IGBT emitter terminal
35	NV	V-phase N-side IGBT emitter terminal
36	NU	U-phase N-side IGBT emitter terminal
37	W	W-phase output terminal
38	V	V-phase output terminal
39	U	U-phase output terminal
40	P	Inverter DC-link positive terminal

No.	Name	Description
2	V <sub>PC</sub>	Internal use (Dummy pin) Don't connect all dummy pins to any other terminals or PCB pattern. (Leave no connect)
5	U <sub>PG</sub>	
8	V <sub>PC</sub>	
11	V <sub>PG</sub>	
17	W <sub>PG</sub>	
20	U <sub>NG</sub>	
30	V <sub>NC</sub>	
31	W <sub>NG</sub>	
32	V <sub>NG</sub>	
33	W	
41	U	
42	V	

**600V LARGE DIIPM Ver.4 Series APPLICATION NOTE**

Table 2-14 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal	$V_{UFB}^-$ $V_{UFS}$	<ul style="list-style-type: none"> <li>Drive supply terminals for P-side IGBTs.</li> <li>By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side <math>V_D</math> supply during ON-state of the corresponding N-side IGBT in the loop.</li> <li>Abnormal operation might happen if the <math>V_D</math> supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such instability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals.</li> <li>Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.</li> </ul>
P-side drive supply GND terminal	$V_{VFB}^-$ $V_{VFS}$ $V_{WFB}^-$ $V_{WFS}$	
P-side control supply terminal	$V_{P1}$ $V_{N1}$	<ul style="list-style-type: none"> <li>Control supply terminals for the built-in HVIC and LVIC.</li> <li>In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals.</li> <li>Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation.</li> <li>It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.</li> </ul>
N-side control supply terminal		
N-side control GND terminal	$V_{PC}$ $V_{NC}$	<ul style="list-style-type: none"> <li>Control ground terminal for the built-in HVIC and LVIC.</li> <li>Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.</li> </ul>
Control input terminal	$U_P, V_P, W_P$ $U_N, V_N, W_N$	<ul style="list-style-type: none"> <li>Control signal input terminals.</li> <li>Voltage input type. These are internally connected to Schmitt trigger circuit..</li> <li>The wiring of each input should be as short as possible to protect the DIIPM from noise interference.</li> <li>Use RC coupling in case of signal oscillation.(Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3k<math>\Omega</math>))</li> </ul>
Sense current detect terminal	$V_{SC}$	<ul style="list-style-type: none"> <li>The sense current split at N-side IGBT flows out from this terminal. For SC protection, connect predefined resistor here.</li> </ul>
Short-circuit trip voltage detecting terminal	CIN	<ul style="list-style-type: none"> <li>Input the potential of <math>V_{SC}</math> terminal (with sense resistor) to CIN terminal for SC protection through RC filter (for the noise immunity).</li> <li>The time constant of RC filter is recommended to be up to 2<math>\mu</math>s.</li> </ul>
Fault signal output terminal	$F_O$	<ul style="list-style-type: none"> <li>Fault signal output terminal for N-side abnormal state(SC or UV).</li> <li>This output is open drain type. <math>F_O</math> signal line should be pulled up to a 5V logic supply with over 5k<math>\Omega</math> resistor (for limiting the <math>F_O</math> sink current <math>I_{F_O}</math> up to 1mA.) Normally 10k<math>\Omega</math> is recommended.</li> </ul>
Fault pulse output width setting terminal	CFO	<ul style="list-style-type: none"> <li>The terminal is for setting the fault pulse output width.</li> <li>An external capacitor should be connected between this terminal and <math>V_{NC}</math>.</li> <li>When 22nF capacitor is connected, then the <math>F_O</math> pulse width becomes 2.4ms.</li> </ul> $C_{FO} = t_{FO} \times 9.1 \times 10^{-6} \text{ (F)}$
Temperature output terminal	$V_{OT}$	<ul style="list-style-type: none"> <li>LVIC temperature is output by analog signal. It is output of OP amplifier internally.</li> </ul>
Inverter DC-link positive terminal	P	<ul style="list-style-type: none"> <li>DC-link positive power supply terminal.</li> <li>Internally connected to the collectors of all P-side IGBTs.</li> <li>To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.</li> </ul>
Inverter DC-link negative terminal	NU, NV, NW	<ul style="list-style-type: none"> <li>Open emitter terminal of each N-side IGBT</li> <li>If usage of common emitter is needed, connect these terminals together at the point as close from the package as possible.</li> </ul>
Inverter power output terminal	U, V, W	<ul style="list-style-type: none"> <li>Inverter output terminals for connection to inverter load (e.g. AC motor).</li> <li>Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.</li> </ul>

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1 $\mu$ s/div. Please ensure the voltage (including surge) not exceed the specified limitation.

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## 2.4 Mounting Method

This section shows the electric spacing and mounting precautions.

### 2.4.1 Electric Spacing

The electric spacing specification of Large DIIPM Ver.4 is shown in Table 2-15

Table 2-15 Minimum insulation distance

	Clearance (mm)	Creepage (mm)
Between live power terminals with high potential	7.1	7.9
Between live control terminals with high potential	3.3	5.6
Between terminals and heat sink	3.7	5.6

### 2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-18. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention to the foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIIPM with the heatsink.

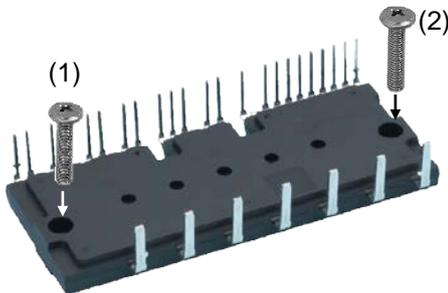


Fig.2-18 Recommended screw fastening order

Temporary fastening  
(1)→(2)  
Permanent fastening  
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.  
Not care the order of fastening (1) or (2), but need to fasten alternately.

Table 2-16 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 1.18N·m, Screw : M4	0.98	-	1.47	N·m
Flatness of outer heat sink	Refer Fig.2-19	-50	-	+100	μm

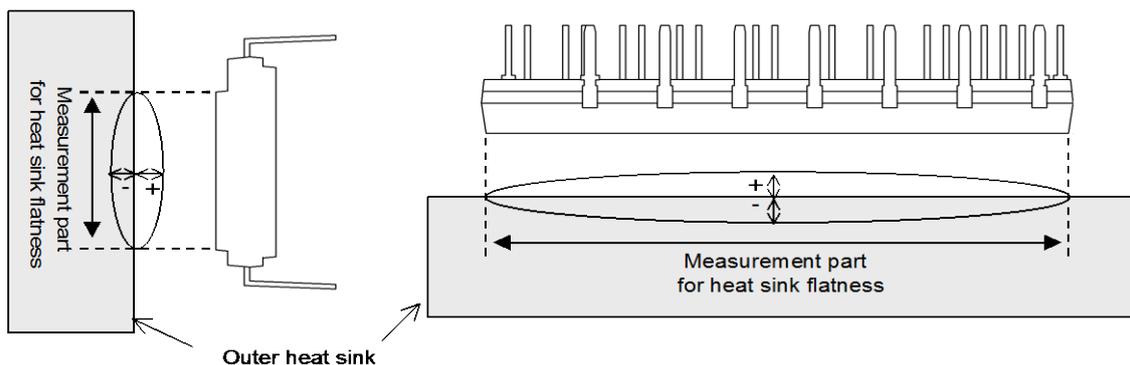


Fig.2-19 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to keep the contact area as large as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp, concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. The contacting thermal resistance between DIIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about 0.2°C/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.  
 (Note: The reflow soldering cannot be recommended for DIIPM.)

### (1) Flow (wave) Soldering

DIIPM is tested on the condition described in Table 2-17 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, and the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-17 Reliability test specification

Item	Condition
Soldering Thermostability	260±5°C, 10±1s

### (2) Hand soldering

Since the temperature impressed upon the DIIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, we cannot suggest the recommended temperature condition for hand soldering.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: Large DIIPM Ver.4

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe.
- (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

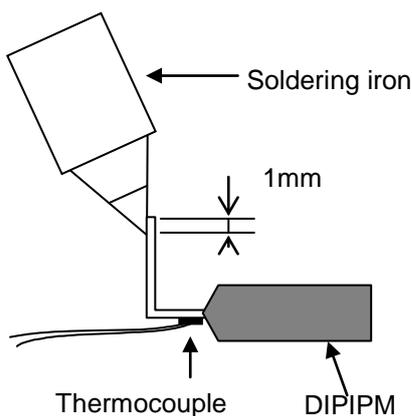


Fig.2-20 Heating and measuring point

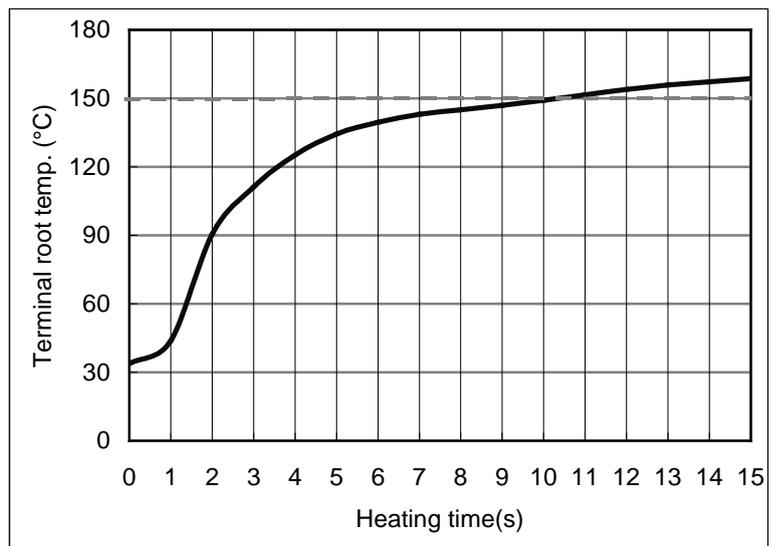


Fig.2-21 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

## CHAPTER3 SYSTEM APPLICATION HIGHLIGHT

### 3.1 Application Guidance

This chapter states usage and interface circuit design hints.

#### 3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics

Note: the capacitance also depends on the PWM control strategy of the application system

C2: 0.22 $\mu$ F ceramic capacitor with good temperature, frequency and DC bias characteristics

C3: 0.1 $\mu$ -0.22 $\mu$ F Film capacitor (for snubber)

D1: Bootstrap diode. High speed type with  $V_{RRM}$  over  $V_{ces}(=600V)$ , trr: up to 100ns

D2: Zener diode 24V/1W for surge absorber

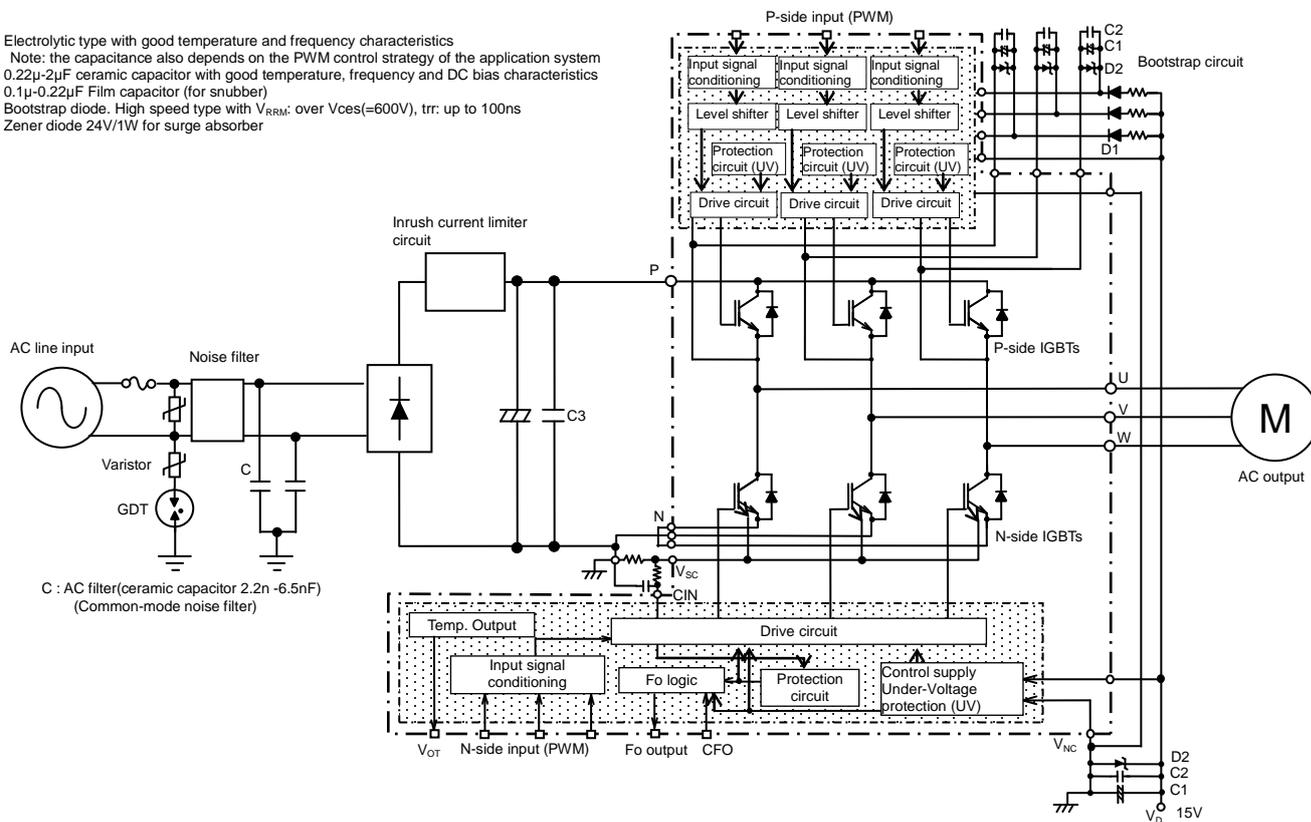


Fig.3-1 Application System block diagram

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.1.2 Interface Circuit (Direct Coupling Interface example)

Fig.3-2 shows a typical application circuit of connecting with MCU or DSP directly.

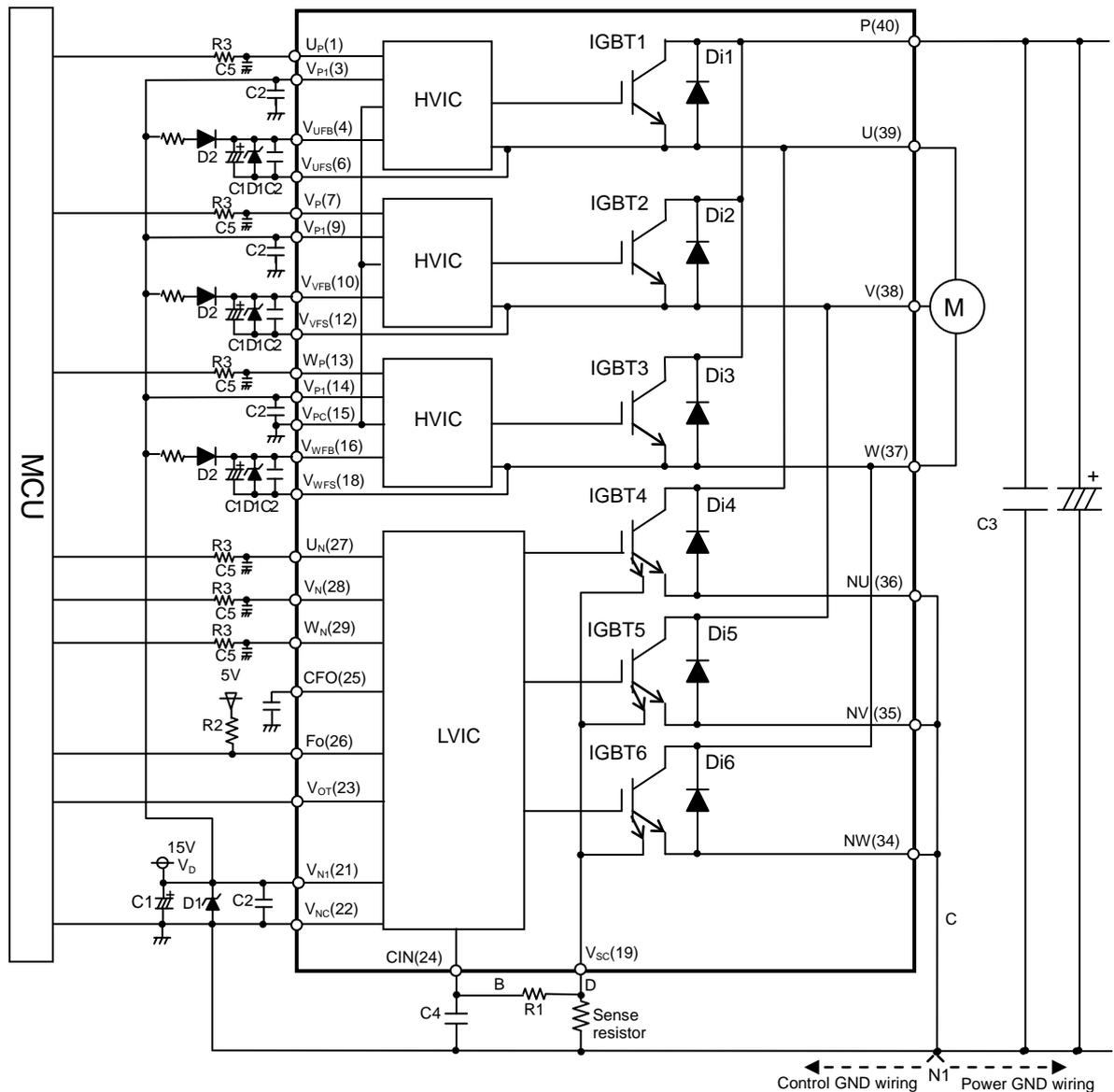


Fig.3-2 Interface circuit example (Direct coupling)

- Note
- 1 :If control GND and power GND are patterned by common wiring, it may cause malfunction by fluctuation of power GND level. It is recommended to connect control GND and power GND at only a N1 point at which NU, NV, NW are connected to power GND line.
  - 2 :It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
  - 3 :To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally inserting a 0.1 $\mu$ ~0.22 $\mu$ F snubber capacitor C3 between the P-N1 terminals is recommended.
  - 4 :R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2 $\mu$ s. (1.5 $\mu$ s~2 $\mu$ s is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is recommended. If R1 is too small, it may leads to delay of protection. So R1 should be min. 10 times larger resistance than Rs. (100 times is recommended.)
  - 5 :To prevent erroneous operation, the wiring of A, B, C should be as short as possible.
  - 6 :For sense resistor, the variation within 1%(including temperature characteristics), low inductance type is recommended. And the over 1/8W is recommended, but it is necessary to evaluate in your real system finally.
  - 7 :To prevent erroneous SC protection, the wiring from V<sub>sc</sub> terminal to CIN filter should be divided at the point D that is close to the terminal of sense resistor. And the wiring should be patterned as short as possible.
  - 8 :All capacitors should be mounted as close to the terminals of the DIIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2: 0.22 $\mu$ ~2.0 $\mu$ F, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
  - 9 :Input drive is High-active type. There is a min. 3.3k $\Omega$  pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be patterned as short as possible. When using RC filter R3C5, it is necessary to confirm the input signal level to meet the turn-on and turn-off threshold voltage. Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
  - 10 :Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes IFo up to 1mA. (IFO is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10k $\Omega$  (5k $\Omega$  or more) is recommended.)
  - 11 :Error signal output width (t<sub>FO</sub>) can be set by the capacitor connected to C<sub>FO</sub> terminal. C<sub>FO</sub>(typ.) = t<sub>FO</sub> x (9.1 x 10<sup>-6</sup>) (F)
  - 12 :High voltage (V<sub>RRM</sub> =600V or more) and fast recovery diode (trr=less than 100ns or less) should be used for D2 in the bootstrap circuit.
  - 13 :If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause erroneous operation. To avoid such problem, voltage ripple of control supply line should meet dV/dt  $\leq$  +/-1V/ $\mu$ s, Vripple $\leq$ 2Vp-p.
  - 14 :For DIIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIIPM.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.1.3 Interface Circuit (Opto-coupler Isolated Interface)

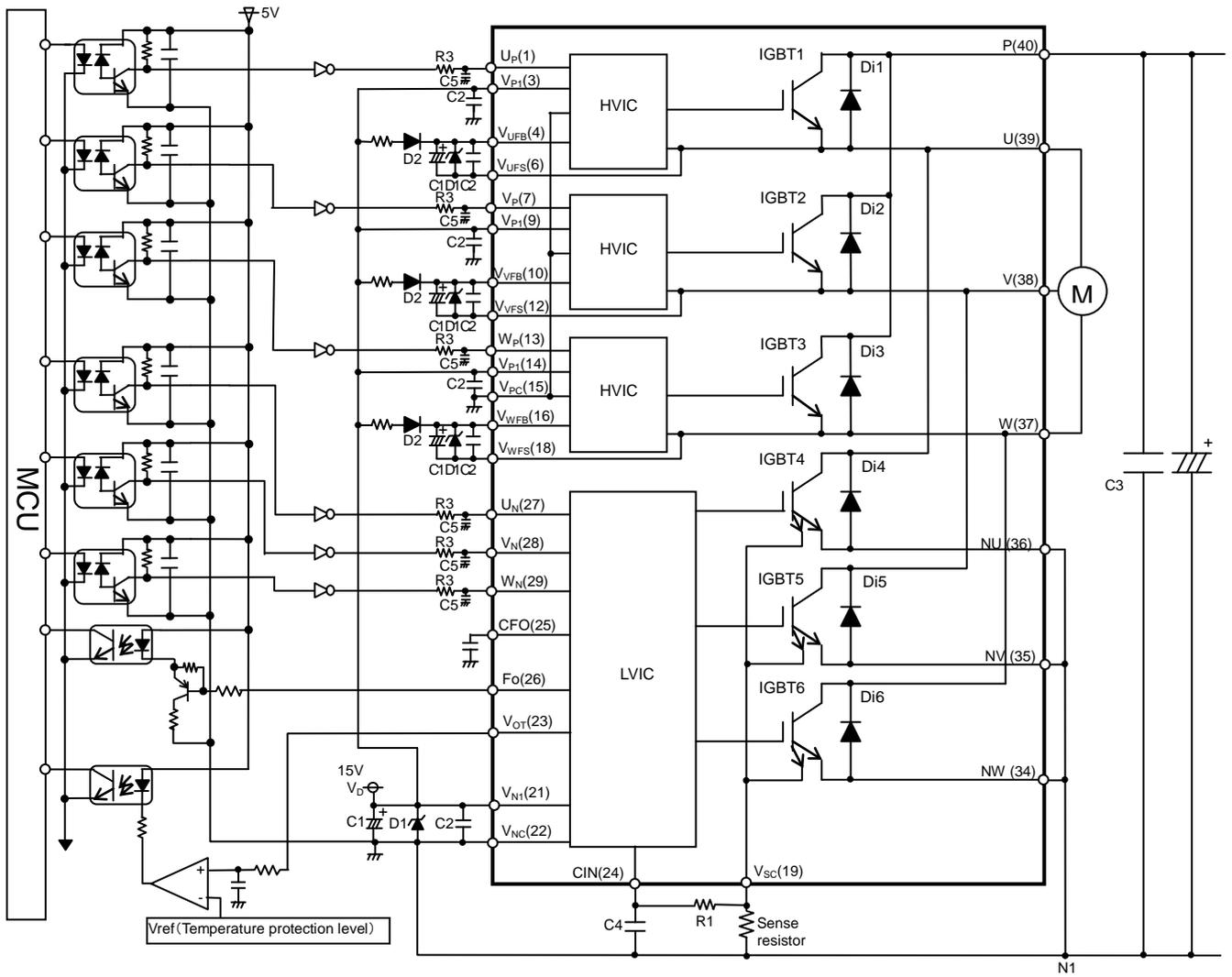


Fig.3-3 Interface circuit example with opto-coupler

**Note:**

- (1) High speed (high CMR) opto-coupler is recommended.
- (2) Fo terminal sink current is max.1mA. A buffer circuit will be necessary to drive an opto-coupler.
- (3) When RC filter R3C5 is inserted for preventing malfunction, it is necessary to confirm the input signal level to meet the turn-on and turn-off threshold voltage.
- (4) About comparator circuit at VOT output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

### 3.1.4 Circuits of Signal Input terminals and Fo Terminal

Large DIIPM Ver.4 is high-active input logic. A 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIIPM as shown in Fig.3-4, so external pull-down resistor is not needed.

When using same PCB for 600V large DIIPM Ver.4 PS21A7\* series and 1200V series PS22A7\* which have same package, it needs to give attention to the difference of input threshold voltage.

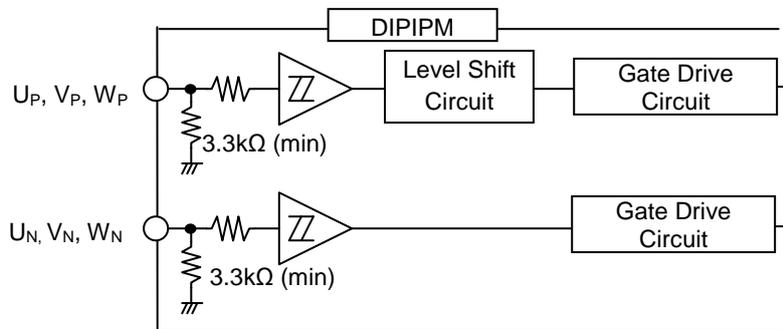


Fig.3-4 Internal structure of control input terminals

Table 3-1 Input threshold voltage ratings ( $T_j=25^\circ\text{C}$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	$V_{th(on)}$	$U_P, V_P, W_P - V_{PC}$	2.1	2.3	2.6	V
Turn-off threshold voltage	$V_{th(off)}$	$U_N, V_N, W_N - V_{NC}$	0.8	1.4	2.1	

The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter.

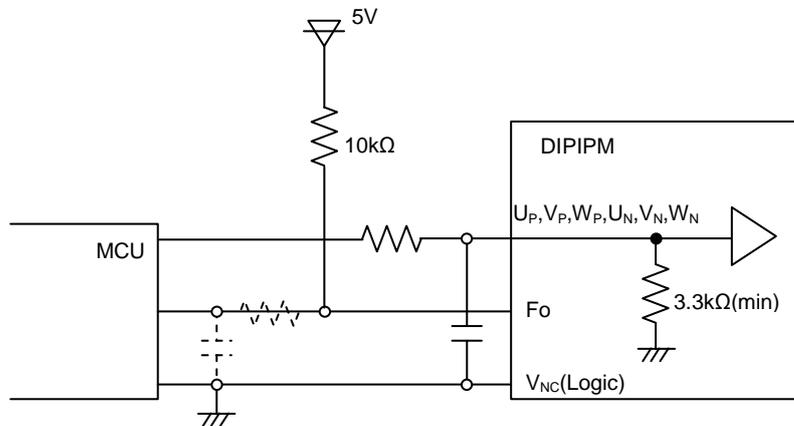


Fig.3-5 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

The DIIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

There are limits for the minimum input pulse width in the DIIPM. The DIIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Please refer Table 3-2)

Table 3-2 Allowable minimum input pulse width

	Symbol	Condition		PN	Min. value	Unit
On signal	PWIN(on)	-		PS21A79	1.1	μs
				PS21A7A	1.3	
Off signal	PWIN(off)	200 ≤ V <sub>CC</sub> ≤ 350V, 13.5 ≤ V <sub>D</sub> ≤ 16.5V, 13.5 ≤ V <sub>DB</sub> ≤ 18.5V, -20 ≤ T <sub>C</sub> ≤ 100°C, N line wiring inductance less than 10nH	Up to rated current	PS21A79	3.0	
				PS21A7A	3.0	
			From rated current to 1.7 times rated current	PS21A79	5.0	
				PS21A7A	5.0	

\*) Input signal with ON pulse width less than PWIN(on) might make no response.

IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer Fig.3-6 about delayed response .

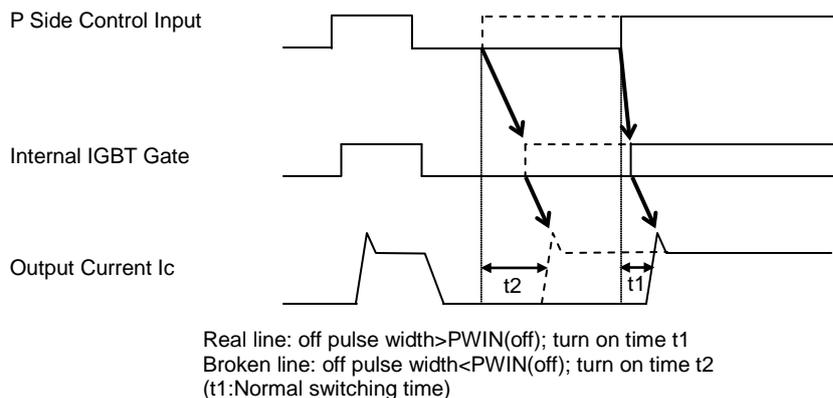


Fig.3-6 Delayed Response with shorter input off (P-side only)

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## (2) Internal Circuit of Fo Terminal

F<sub>O</sub> terminal is an open drain type, it should be pulled up to control supply (e.g. 5V) as shown in Fig.3-5. Fig.3-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. (I<sub>Fo</sub> can be estimated from I<sub>Fo</sub>=control supply voltage / pull up resistance approximately.) If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-3 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V <sub>FOH</sub>	V <sub>SC</sub> =0V, Fo=10kΩ, 5V pulled-up	4.9	-	-	V
	V <sub>FOL</sub>	V <sub>SC</sub> =1V, Fo=1mA	-	-	0.95	V

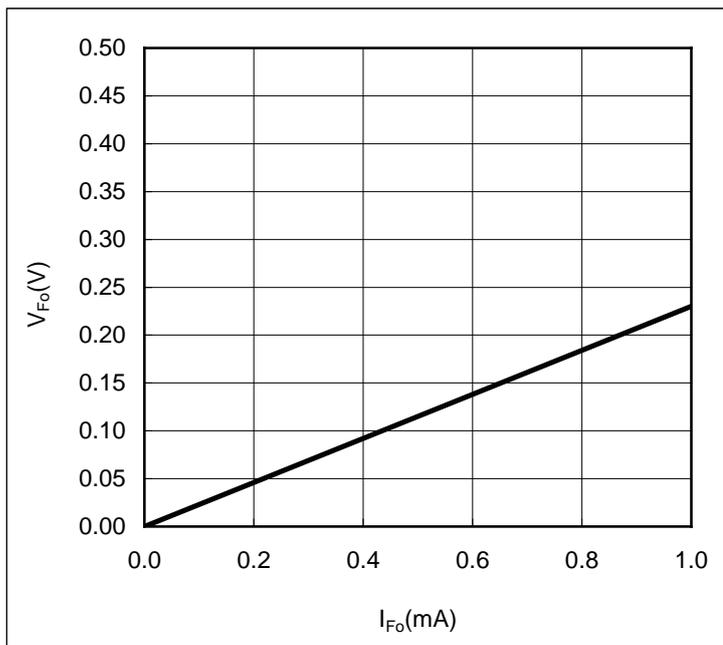


Fig.3-7 Fo terminal typical V-I characteristics (V<sub>D</sub>=15V, T<sub>j</sub>=25°C)

### 3.1.5 Snubber Circuit

In order to prevent DIIPM from the surge destruction, the wiring length between the smoothing capacitor and DIIPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted to the position between P and the connect point of NU, NV and NW terminals as close as possible as Fig.3-8.

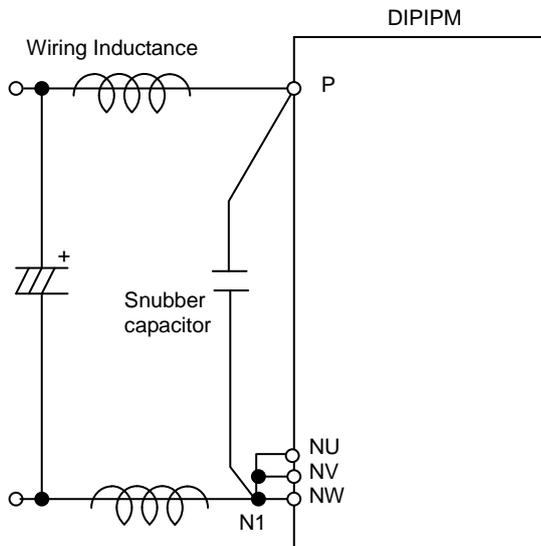


Fig.3-8 Recommended snubber circuit position



# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.1.7 Precaution for wiring on PCB

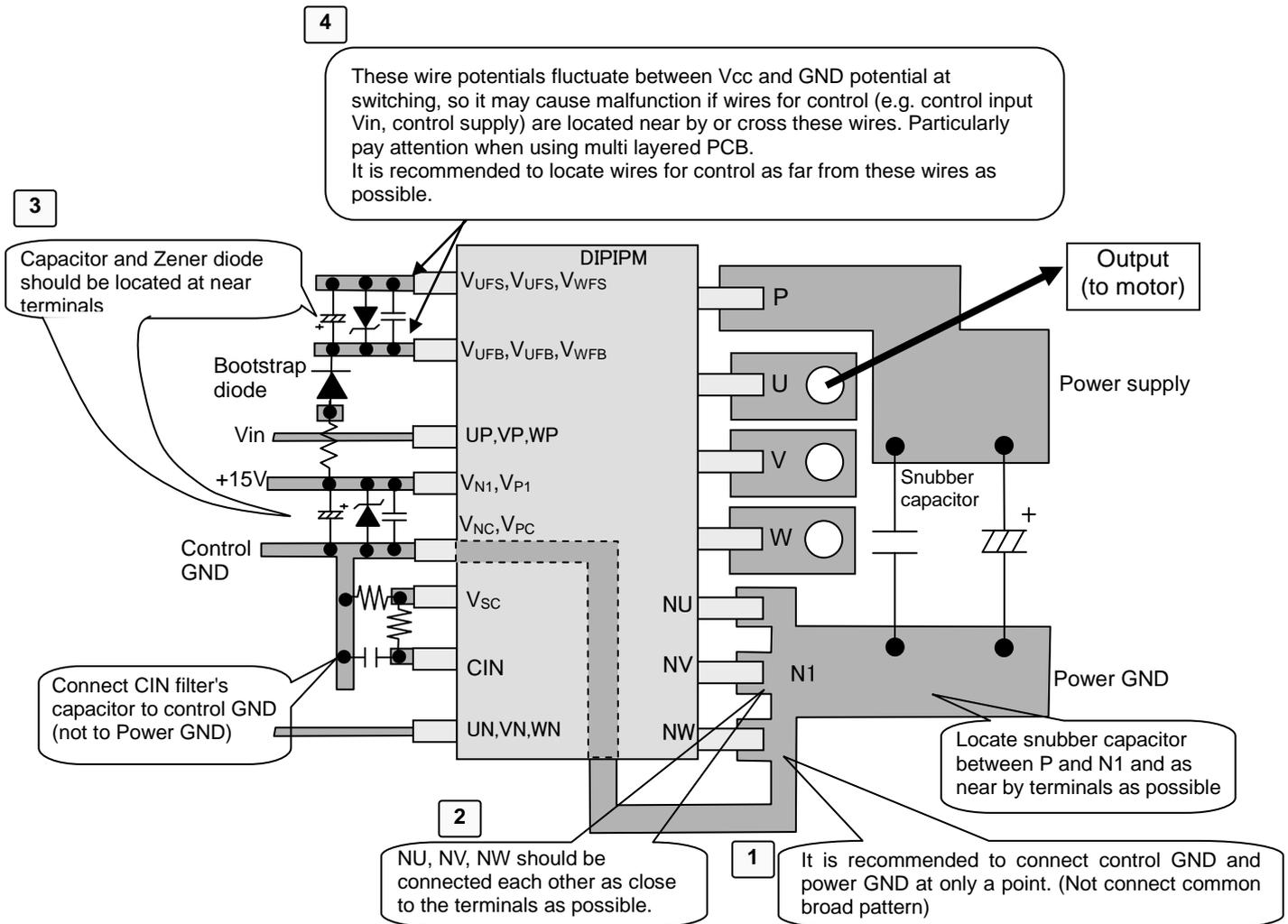


Fig.3-10 Precaution for wiring on PCB

### The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. it causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Finally the arm short occurs.
	•Ground loop pattern is existing.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short occurs.
2	•Long pattern between NU, NV, NW terminals and N1	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction by VS voltage (output terminal potential) decreasing excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction occurs.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	The cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIIPM. Then since the incorrect signals are input to DIIPM, the arm short circuit might occur.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.1.8 SOA of DIIPM

The following describes the SOA (Safety Operating Area) of DIIPM.

- $V_{CES}$  : Maximum rating of IGBT collector-emitter voltage
- $V_{CC}$  : Supply voltage applied on P-N terminals
- $V_{CC(surge)}$ : The total amount of  $V_{CC}$  and the surge voltage generated by the wiring inductance and the DC-link capacitor.
- $V_{CC(PROT)}$  : DC-link voltage that DIIPM can protect itself.

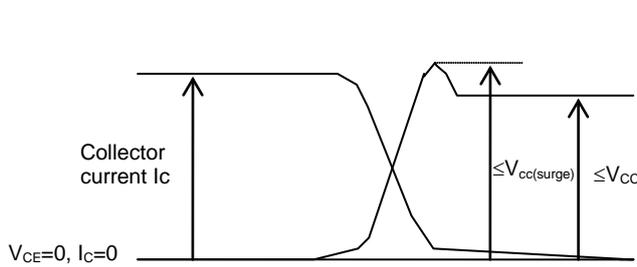


Fig.3-11 SOA at switching mode

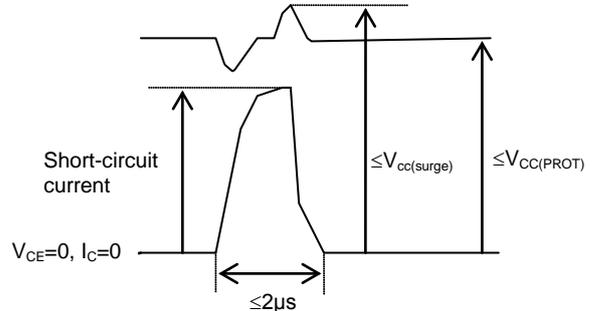


Fig.3-12 SOA at short-circuit mode

### In Case of switching

$V_{CES}$  represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from  $V_{CES}$  is  $V_{CC(surge)}$ , that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIIPM and DC-link capacitor from  $V_{CC(surge)}$  derives  $V_{CC}$ , that is 450V.

### In Case of Short-circuit

$V_{CES}$  represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from  $V_{CES}$  is  $V_{CC(surge)}$ , that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIIPM and the electrolytic capacitor from  $V_{CC(surge)}$  derives  $V_{CC}$ , that is, 400V.

## 3.1.9 SCSOA

Fig.3-13 and Fig.3-14 show the typical SCSOA performance curves of PS21A7A and PS21A79.

Conditions:  $V_{cc}=400V$ ,  $T_j=125^\circ C$  at initial state,  $V_{cc(surge)} \le 500V$  (surge included), non-repetitive, 2m load.

The DIIPM can shutdown safely an SC current that is about 10 times of its current rating under the conditions only if the IGBT conducting period is less than 4.5 $\mu sec$ .

Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

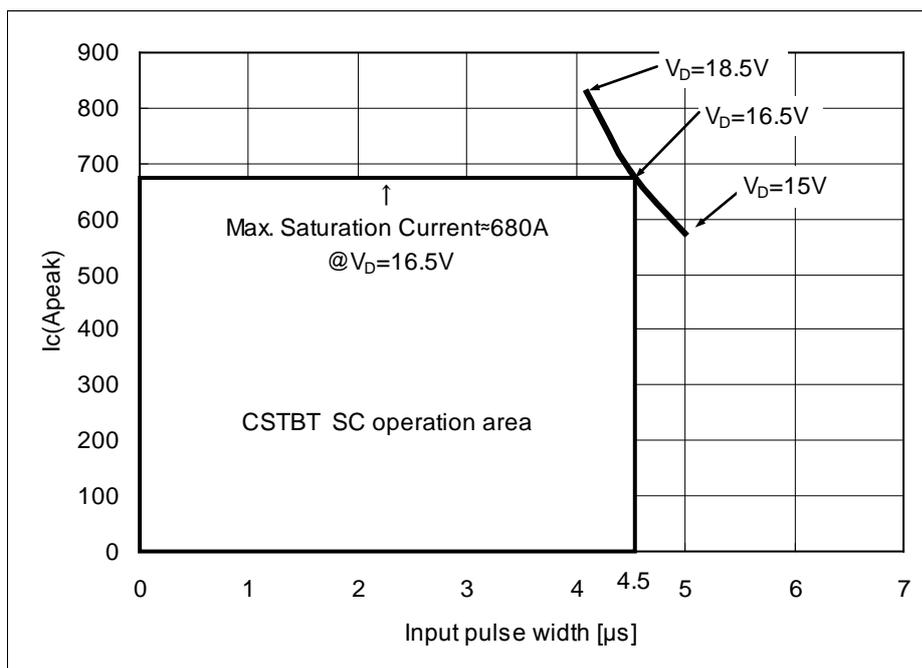


Fig.3-13 PS21A7A typical SCSOA curve

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

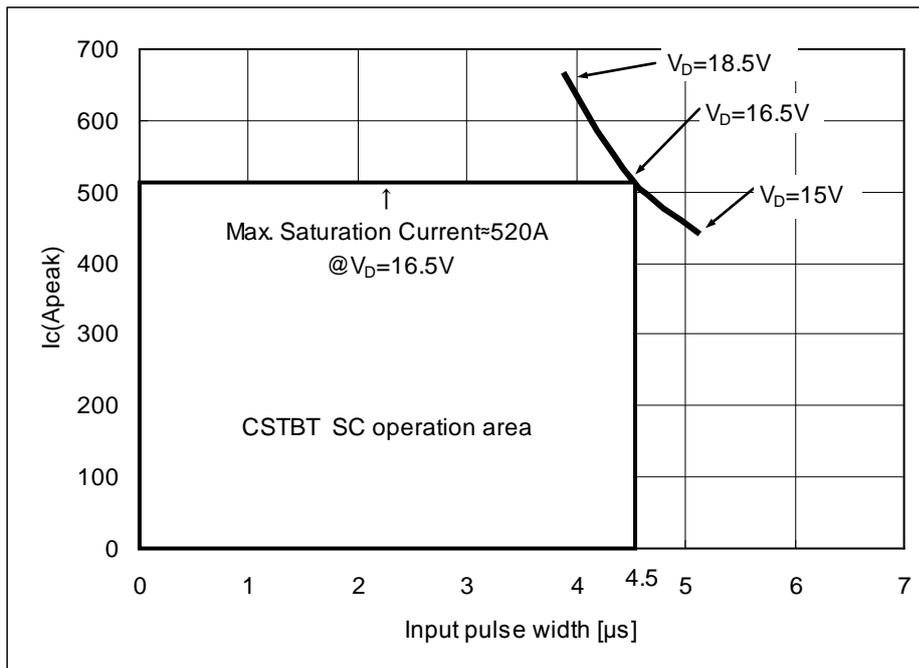


Fig.3-14 PS21A79 typical SCSOA curve

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

### 3.1.10 Power Life Cycles

When DIIPM is in operation, repetitive temperature variation will happen on the IGBT junctions ( $\Delta T_j$ ). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-15 shows the IGBT power cycle curve as a function of average junction temperature variation ( $\Delta T_j$ ).

(The curve is a regression curve based on 3 points of  $\Delta T_j=46, 88, 98K$  with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

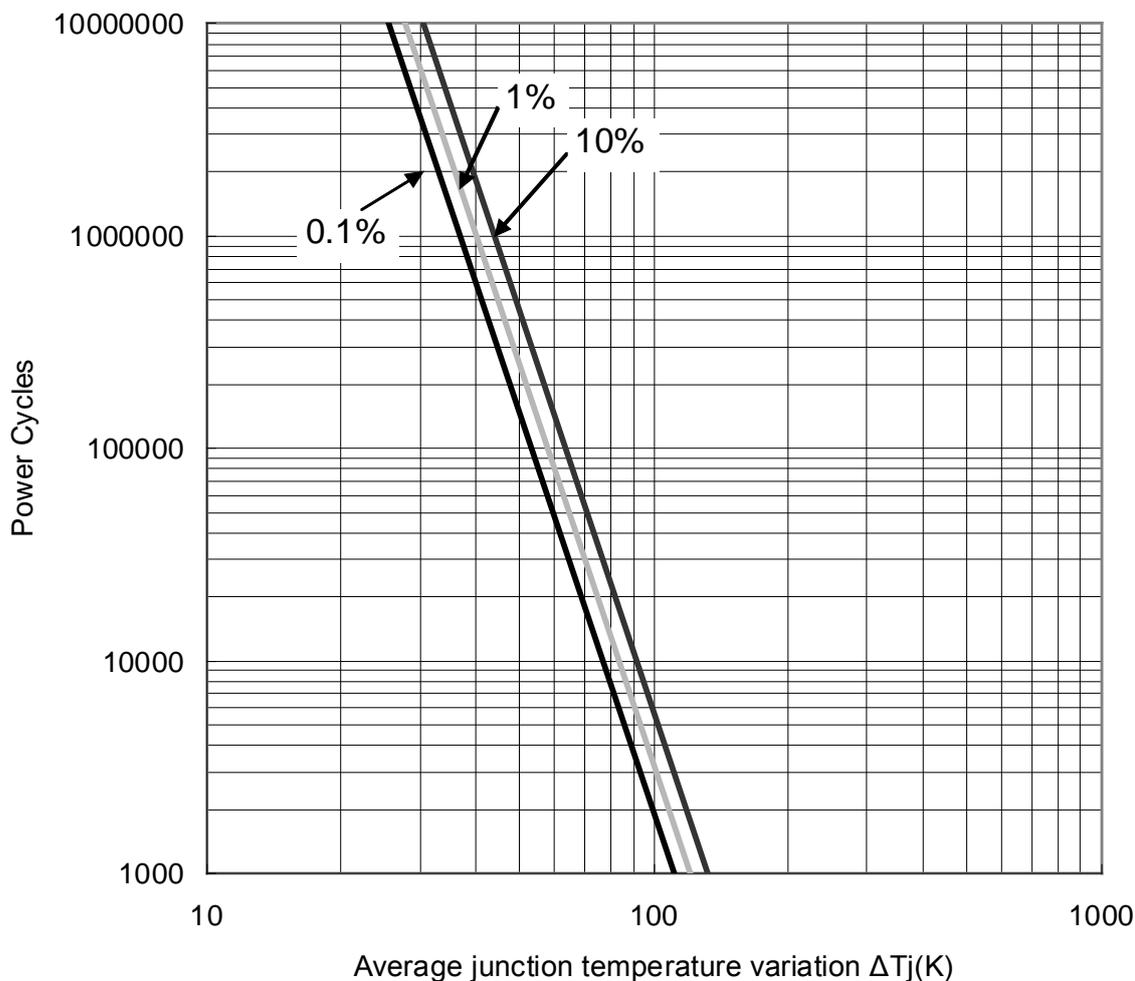


Fig.3-15 Power cycle curve

## 3.2 Power Loss and Thermal Dissipation Calculation

### 3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

- (a) PWM controlled VVVF inverter with sinusoidal output;
- (b) PWM signals are generated by the comparison of sine waveform and triangular waveform.
- (c) Duty amplitude of PWM signals varies between  $\frac{1-D}{2} \sim \frac{1+D}{2}$  (%/100), (D: modulation depth).
- (d) Output current varies with  $I_{cp} \cdot \sin x$  and it does not include ripple.
- (e) Power factor of load output current is  $\cos\theta$ , ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle  $x$  as  $\frac{1+D \times \sin x}{2}$  which is equivalent to the output voltage variation. From the power factor  $\cos\theta$ , the output current and its corresponding PWM duty at any phase angle  $x$  can be obtained as below:

$$\begin{aligned} \text{Output current} &= I_{cp} \times \sin x \\ \text{PWM Duty} &= \frac{1 + D \times \sin(x + \theta)}{2} \end{aligned}$$

Then,  $V_{CE(sat)}$  and  $V_{EC}$  at the phase  $x$  can be calculated by using a linear approximation:

$$\begin{aligned} V_{ce(sat)} &= V_{ce(sat)}(@ I_{cp} \times \sin x) \\ V_{ec} &= (-1) \times V_{ec}(@ I_{cp}(= I_{cp}) \times \sin x) \end{aligned}$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi} \int_0^\pi (I_{cp} \times \sin x) \times V_{ce(sat)}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi} \int_\pi^{2\pi} ((-1) \times I_{cp} \times \sin x) ((-1) \times V_{ec}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2}) \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi} \int_0^\pi (P_{sw(on)}(@ I_{cp} \times \sin x) + P_{sw(off)}(@ I_{cp} \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-16, and its dynamic loss can be calculated by the following expression:

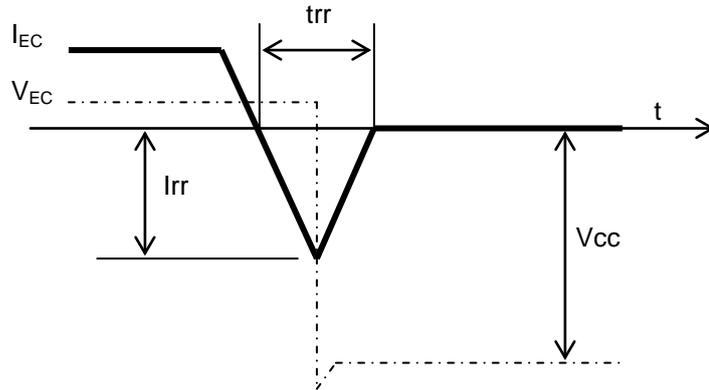


Fig.3-16 Ideal FWDi recovery characteristics curve

$$P_{sw} = \frac{I_{rr} \times V_{cc} \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times trr(@ I_{cp} \times \sin x)}{4} \times fc \cdot dx \\ & = \frac{1}{8} \int_{\rho}^{2\pi} I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times trr(@ I_{cp} \times \sin x) \times fc \cdot dx \end{aligned}$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current,  $V_{CE(sat)}$ ,  $V_{EC}$ , and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$ ,  $V_{EC}$  and Psw(on, off) should be the values at  $T_j=125^{\circ}C$ .

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-17 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions:  $V_{CC}=300V$ ,  $V_D=V_{DB}=15V$ ,  $V_{CE(sat)}=Typ.$ ,  $P.F=0.8$ ,  $Switching\ loss=Typ.$ ,  $T_j=125^\circ C$ ,  $T_c=100^\circ C$ ,  $R_{th(j-c)}=Max.$ , 3-phase PWM modulation, 60Hz sine waveform output

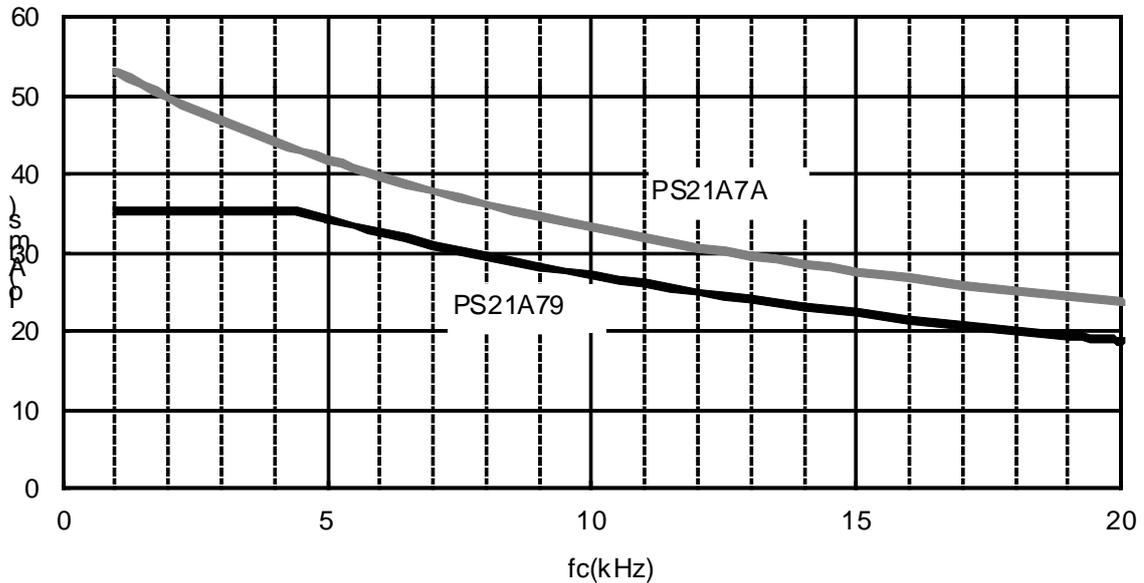


Fig.3-17 Effective current-carrier frequency characteristic

Fig.3-17 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ( $T_c=100^\circ C$  and  $T_j=125^\circ C$ ). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The inverter loss can be calculated from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: <http://www.mitsubishielectric.com/semiconductors/>).

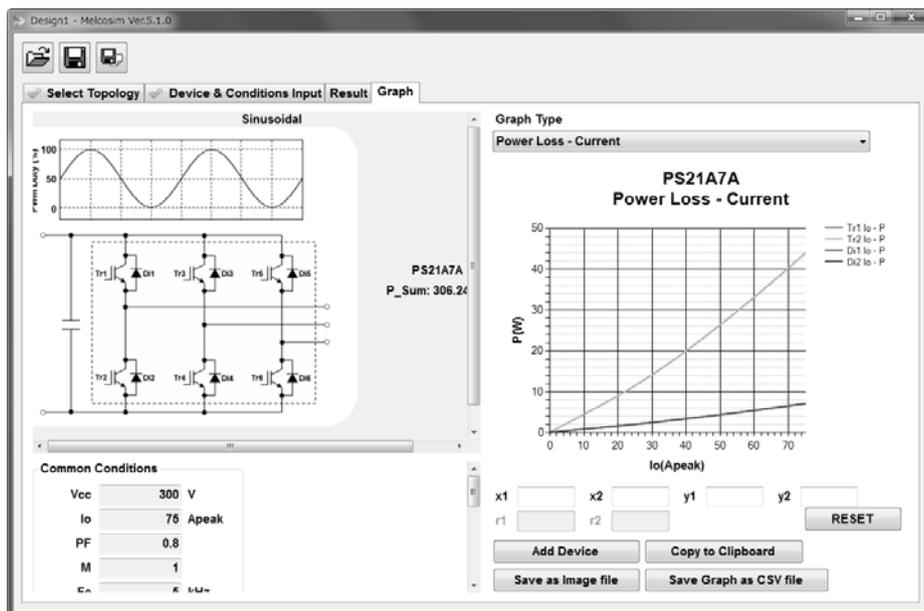


Fig.3-18 Loss simulator screen image

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

## 3.3 Noise Withstand Capability

### 3.3.1 Evaluation Circuit

DIIPM have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-19. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

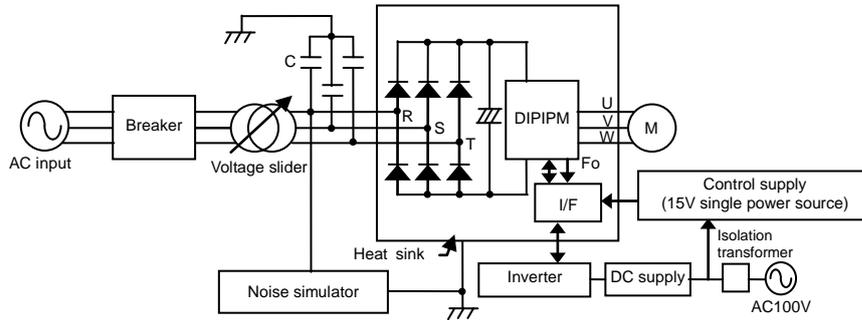


Fig.3-19 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers  
15V single power supply, Test is performed with IM

#### Test conditions

$V_{CC}=300V$ ,  $V_D=15V$ ,  $T_a=25^\circ C$ , no load

Scheme of applying noise: From AC line (R, S, T), Period  $T=16ms$ , Pulse width  $t_w=0.05-1\mu s$ , input in random.

### 3.3.2 Countermeasures and Precautions

DIIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIIPM (due to no good wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, the countermeasures are recommended.

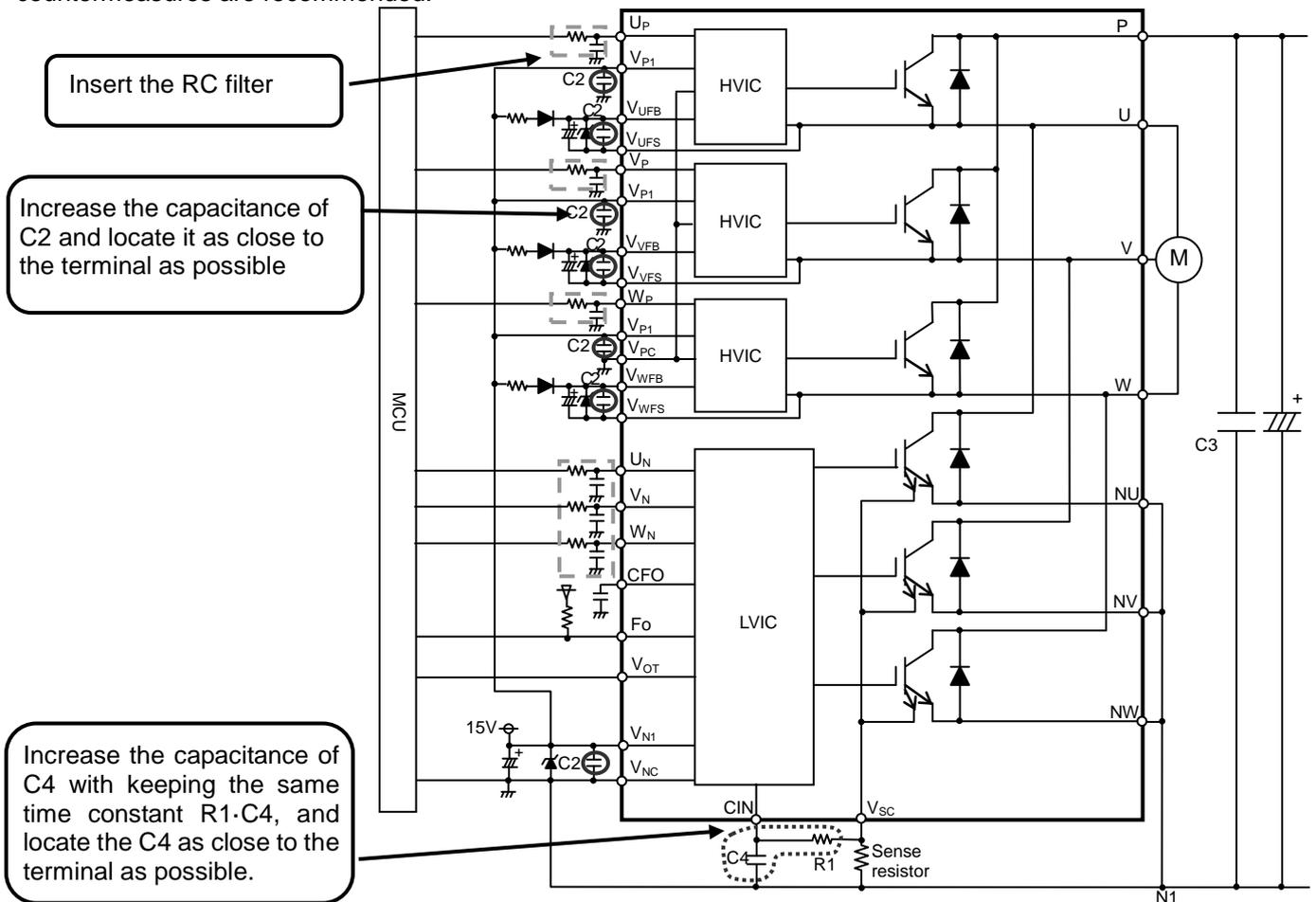


Fig.3-20 Example of countermeasures

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

### 3.3.3 Static Electricity Withstand Capability

DIIPM has been confirmed to be with +/-200V or more typical withstand capability against static electricity from the following tests shown in Fig.3-21 and Fig.3-22. The results are described in Table 3-4

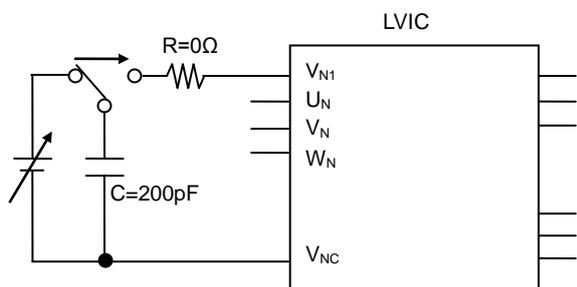


Fig.3-21  $V_{N1}$  terminal Surge Test circuit( $V_{N1}$  terminal)

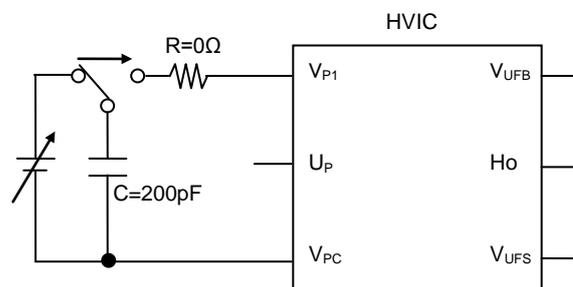


Fig.3-22  $V_{P1}$  terminal Surge Test circuit( $V_{P1}$  terminal)

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage.  
(Limit voltage of surge simulator:  $\pm 4.0\text{kV}$ , Judgment method; change in V-I characteristic)

Table 3-4 Typical ESD capability for PS21A7A and PS21A79 (typical data)

[Control terminal part]

For control part, since both have same circuit in the control IC, they have same capability.

Terminals	+	-
UP, VP, WP- $V_{PC}$	1.6	1.7
$V_{P1} - V_{NC}$	3.6	3.7
$V_{UFB} - V_{UFS}$ , $V_{VFB} - V_{VFS}$ , $V_{WFB} - V_{WFS}$	4.0 or more	4.0 or more
UN, VN, WN- $V_{NC}$	0.7	1.6
$V_{N1} - V_{NC}$	4.0 or more	4.0 or more
CIN- $V_{NC}$	0.8	1.0
FO- $V_{NC}$	1.5	2.4
CFO- $V_{NC}$	1.3	1.7
$V_{OT} - V_{NC}$	0.9	2.5

[Power terminal part for PS21A7A]

Terminals	+	-
$V_{SC} - V_{NC}^*$	0.4	0.5
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

[Power terminal part for PS21A79]

Terminals	+	-
$V_{SC} - V_{NC}^*$	0.5	1.1
P-NU, NV, NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

\*  $V_{SC}$  terminal (IGBT sense) is connected to the power chip inside the module.

## CHAPTER 4 Bootstrap Circuit Operation

### 4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor.

It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC, limiting resistance and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

The circuit current characteristics in switching situation of P-side IGBT are described below.

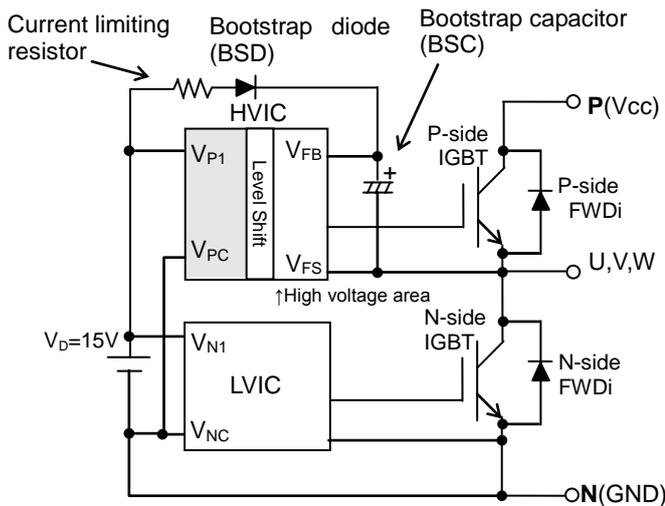


Fig.4-1 Bootstrap Circuit Diagram

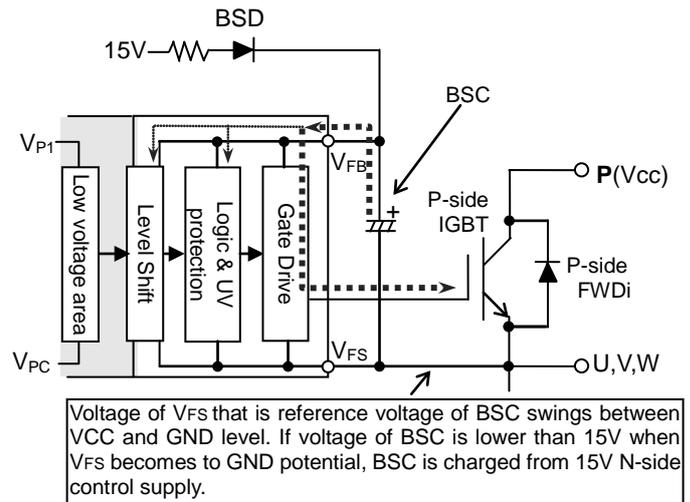


Fig.4-2 Bootstrap Circuit Diagram

Voltage of V<sub>FS</sub> that is reference voltage of BSC swings between V<sub>CC</sub> and GND level. If voltage of BSC is lower than 15V when V<sub>FS</sub> becomes to GND potential, BSC is charged from 15V N-side control supply.

## 4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current  $I_{DB}$  at steady state is maximum 0.55mA for 600V Large DIIPM Ver.4 series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current will exceed 0.55mA and increases proportional to carrier frequency. For reference, Fig.4-3~4-4 show the circuit current  $I_{DB}$  for P-side IGBT driving supply - carrier frequency  $f_c$  typical characteristics for each products. (Conditions:  $V_D=V_{DB}=15V$ ,  $T_j=125^\circ C$ , IGBT ON Duty=10, 30, 50, 70, 90%)

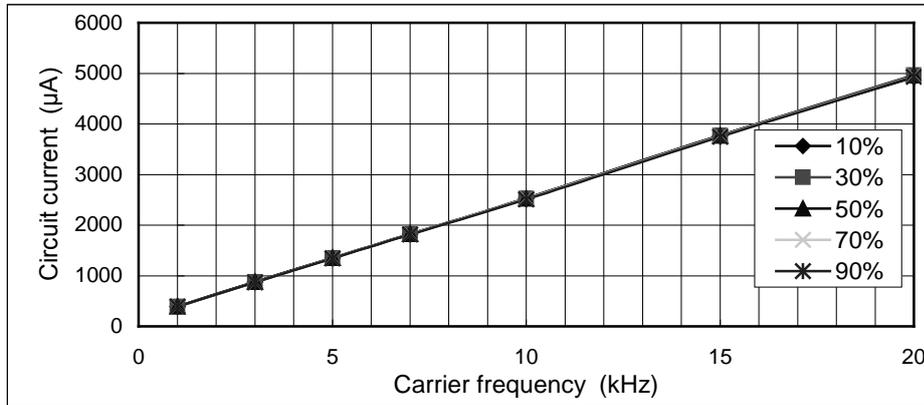


Fig.4-3  $I_{DB}$  vs. Carrier frequency for PS21A7A

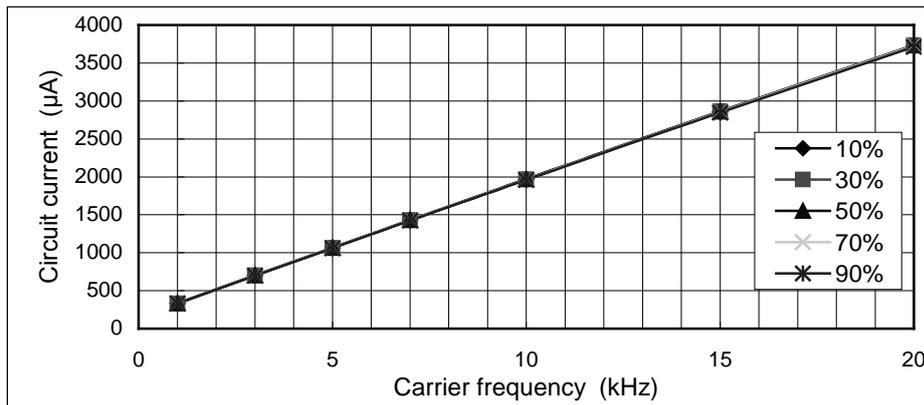


Fig.4-4  $I_{DB}$  vs. Carrier frequency for PS21A79

## 4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

### (1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-1.

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

# 600V LARGE DIIPM Ver.4 Series APPLICATION NOTE

Table 4-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	<ul style="list-style-type: none"> <li>Aluminum type: Low temp.: -10% High temp: +10%</li> <li>Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%</li> </ul>	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

### (2) Bootstrap diode

It is recommended for BSD to have same or higher blocking voltage with collector-emitter voltage  $V_{CES}$  of IGBT in DIIPM. (i.e. 600V or more is needed in the case of 600V DIIPM.) And its recovery time  $t_{rr}$  should be less than 100ns. (Fast recovery type)

Also **it is highly recommended to apply the high quality product such as small variations of blocking voltage.** If BSD broke by impressed overvoltage and shorted, it leads to the control ICs over voltage destruction because DC-link voltage ( $V_{cc}$ ) is impressed upon low voltage area of control ICs. Then DIIPM will lose various functions like protection and gate driving and it may lead to serious system destruction.

### (3) Current limiting resistor

When designing limiting resistor, it is important to note its power rating, surge withstand capability (there is the possibility that surge may be impressed on the resistor when switching ON or OFF timing) and so on.

Especially if small chip type resistor is applied, it is recommended to select anti-surge designed type. For detailed information, please refer to the resistor manufacturer.

## 4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

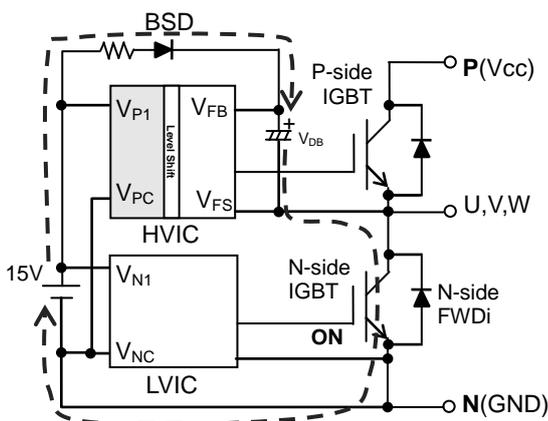


Fig.4-5 Initial charging root

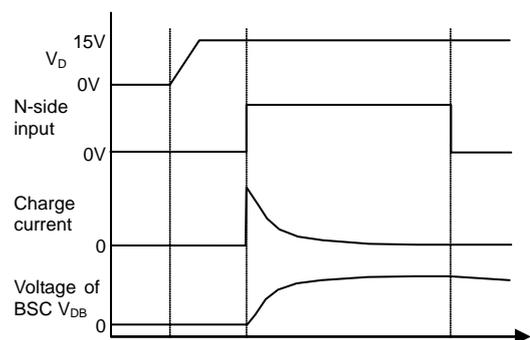


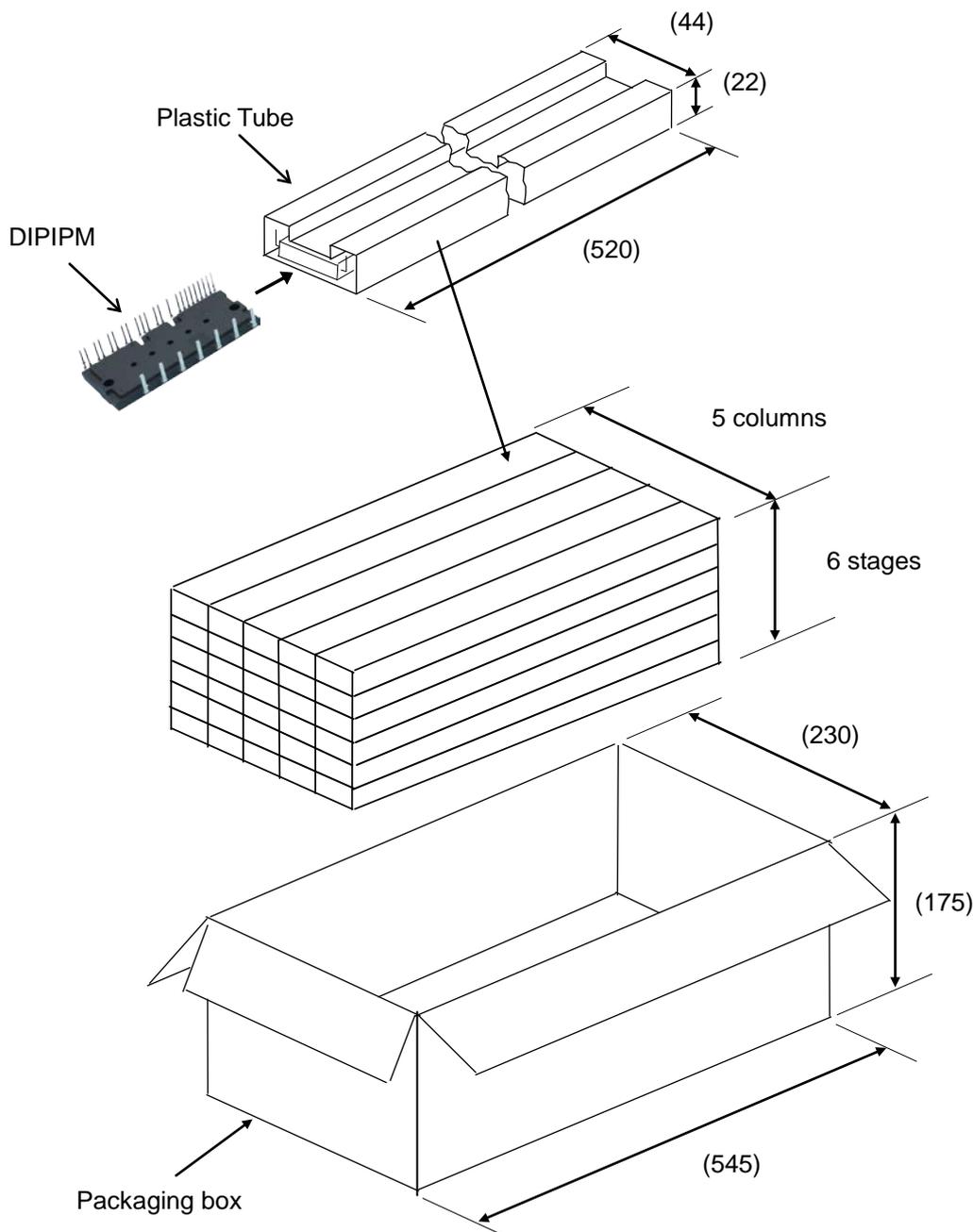
Fig.4-6 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width  $PW_{IN(on)}$ . (e.g. 1.3µs or more for PS21A7A. Refer the datasheet for each product.)

## CHAPTER5 PACKAGE HANDLING

### 5.1 Packaging Specification



Quantity:  
6pcs per 1 tube

Total amount in one box (max):  
Tube Quantity: 5 × 6=30pcs  
IPM Quantity: 30 × 6=180pcs

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):  
About 46g per 1pcs  
About 380g per 1tube  
About 13kg per 1box

Spacers are inserted into the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

## 5.2 Handling Precautions

# Cautions

Transportation	<ul style="list-style-type: none"><li>•Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged.</li><li>•Throwing or dropping the packaging boxes might cause the devices to be damaged.</li><li>•Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.</li></ul>
Storage	<ul style="list-style-type: none"><li>•We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.</li></ul>
Long storage	<ul style="list-style-type: none"><li>•When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.</li></ul>
Surroundings	<ul style="list-style-type: none"><li>•Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.</li></ul>
Flame resistance	<ul style="list-style-type: none"><li>•The epoxy resin of case material is flame-resistant type (UL standard 94V-0), but they are not noninflammable.</li></ul>
Static electricity	<ul style="list-style-type: none"><li>•ICs and power chips with MOS gate structure are used for the DIIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity.</li></ul> <p>(1) Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none"><li>*Containers that charge static electricity easily should not be used for transit and for storage.</li><li>*Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands.</li><li>*Should not be taking out DIIPM from tubes until just before using DIIPM and never touch terminals with bare hands.</li><li>*During assembly and after taking out DIIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats.</li><li>*When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board.</li><li>*If using a soldering iron, earth its tip.</li></ul> <p>(2) Notice when the control terminals are open</p> <ul style="list-style-type: none"><li>*When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction.</li><li>*Short the terminals before taking a module off.</li></ul>

## Revision Record

Rev.	Date	Revised Points
1	08/31/2011	New
2	10/15/2012	<ul style="list-style-type: none"><li>· Fig.2-11 <math>V_{OT}</math> output vs. LVIC temperature</li><li>· Table 2-14 Detailed description of input and output terminals</li><li>· Section 3.1.2 Interface Circuit (Direct Coupling Interface example)</li><li>· Section 3.1.3 Interface Circuit (Opto-coupler Isolated Interface)</li><li>· Chapter 4 Bootstrap Circuit operation</li></ul>
3	1/ 6/2014	<ul style="list-style-type: none"><li>· Section 2.4.2</li><li>· Add Fig.3-18</li><li>· Add section 4.4</li></ul>

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